High-Temperature Single-Crystal 3C-SiC Capacitive Pressure Sensor

Darrin J. Young, *Member, IEEE*, Jiangang Du, Christian A. Zorman, *Member, IEEE*, and Wen H. Ko, *Life Fellow, IEEE*

***Abstract*—Single-crystal 3C-silicon carbide (SiC) capacitive pressure sensors are proposed for high-temperature sensing applications. The prototype device consists of an edge-clamped circular 3C-SiC diaphragm with a radius of 400 μm and a thickness of 0.5 μm suspended over a 2-μm sealed cavity on a silicon substrate. The 3C-SiC film is grown epitaxially on a 100-mm diameter $\langle 100 \rangle$ silicon substrate by atmospheric pressure chemical vapor deposition. The fabricated sensor demonstrates a high-temperature sensing capability up to 400 °C, limited by the test setup. At 400 °C, the device achieves a linear characteristic response between 1100 and 1760 torr with a sensitivity of 7.7 fF/torr, a linearity of 2.1%, and a hysterisis of 3.7% with a sensing repeatability of 39 torr (52 mbar). A wide range of sensor specifications, such as linear ranges, sensitivities, and capacitance values, can be achieved by choosing the proper device geometrical parameters.**

***Index Terms*—Capacitive sensor, high-temperature sensor, pressure, silicon carbide (SiC).**

I. INTRODUCTION

HIGH-TEMPERATURE pressure sensors are critical for advanced industrial, automotive, and aerospace sensing applications. Typical temperatures for these applications range from 200–600 °C. Silicon pressure sensors based on piezoresistive and capacitive sensing schemes have been developed [1]–[3]. However, silicon structures suffer from severe mechanical performance degradation above 500 °C and, thus, are inadequate for building reliable high-temperature sensors. Silicon carbide (SiC) is an attractive material for high-temperature applications because of its mechanical robustness, chemical inertness, and electrical stability at elevated temperatures, and, thus, sensors made of SiC are expected to perform reliably well above 500 °C [4]. High-temperature pressure sensors have been proposed and implemented using SiC-based piezoresistive devices and have demonstrated sensing capabilities between 350 and 600 °C [5]–[7]. Piezoresistive sensors, however, exhibit a strong temperature dependence and suffer from contact resistance variations at elevated temperatures, substantially degrading the sensor performance because the contact resistance variation is indistinguishable from the piezoresistance change caused by the pressure to be sensed. Capacitive pressure sensors are attractive for high-temperature applications because the device performance is tolerant of contact resistance variations and wireless sensing schemes can be readily realized [8], [9] to eliminate any potential performance degradation due to wiring parasitic capacitances. Furthermore, capacitive devices can achieve a high sensitivity, low turn-on temperature drift, and a minimum dependence on side stress and other environmental variations.

In this paper, a single-crystal 3C-SiC capacitive pressure sensor is presented. Single-crystal 3C-SiC material is chosen because it is available in current fabrication facility and can be readily grown on a 4″ silicon wafer surface with a controlled quality. Other SiC materials, such as 4H-SiC and 6H-SiC thin films, can also be used to fabricate high-temperature capacitive pressure sensors. The prototype device demonstrates a sensing capability up to 400 °C, the highest temperature performance of semiconductor capacitive pressure sensors to date. The achieved performance is suitable for various high-temperature sensing applications. In Section II, the proposed capacitive pressure sensor architecture and operating principles are presented. Single-crystal 3C-SiC thin-film growth technology with film quality characterization is illustrated in Section III. Section IV outlines the proposed capacitive sensor fabrication process with device measurement results shown in Section V.

II. SiC CAPACITIVE PRESSURE SENSOR

Fig. 1 presents a simplified cross-sectional view of the proposed capacitive pressure sensor. The device consists of an edge-clamped circular 3C-SiC diaphragm suspended over a sealed cavity on a silicon substrate. The diaphragm deflects toward the substrate under an increasing external pressure, thus increasing the device capacitance value between the diaphragm and substrate. Once the diaphragm touches the substrate at a designed touch point pressure $(\mathrm{P_T})$, the sensor capacitance increases near linearly with pressure due to the linearly increasing touched area [2]. Fig. 2 illustrates a typical device characteristic response between the sensor capacitance value and applied pressure. The nearly linear behavior is desirable for various sensing applications. Single-crystal 3C-SiC material is chosen for the bending diaphragm because it can be readily grown on a 4″ silicon wafer surface with a controlled quality as will be illustrated in the following section, thus ensuring reliable performance at elevated temperatures.

The sensor diaphragm thickness and radius, cavity depth, and dielectric layer thickness can be designed to obtain various touch point pressures, linear ranges, sensitivities, and sensor capacitance values. The $\mathrm{P_T}$ of an edge clamped circular

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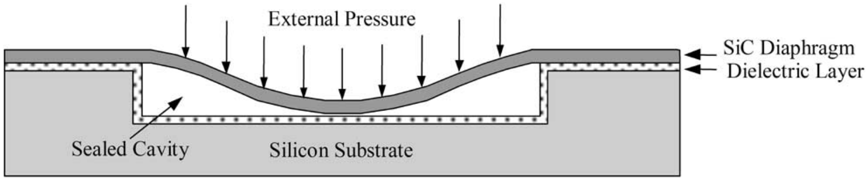

Fig. 1. SiC pressure sensor cross-sectional view.

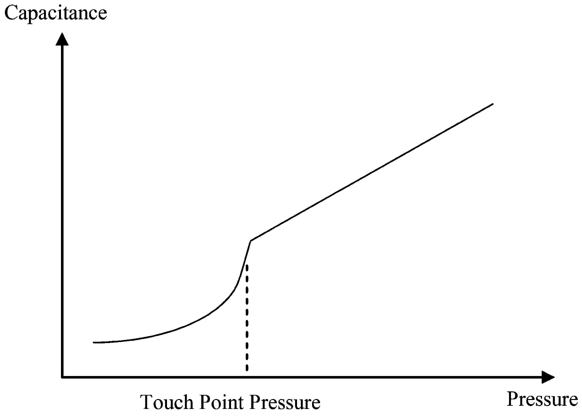

Fig. 2. Pressure sensor characteristic response.

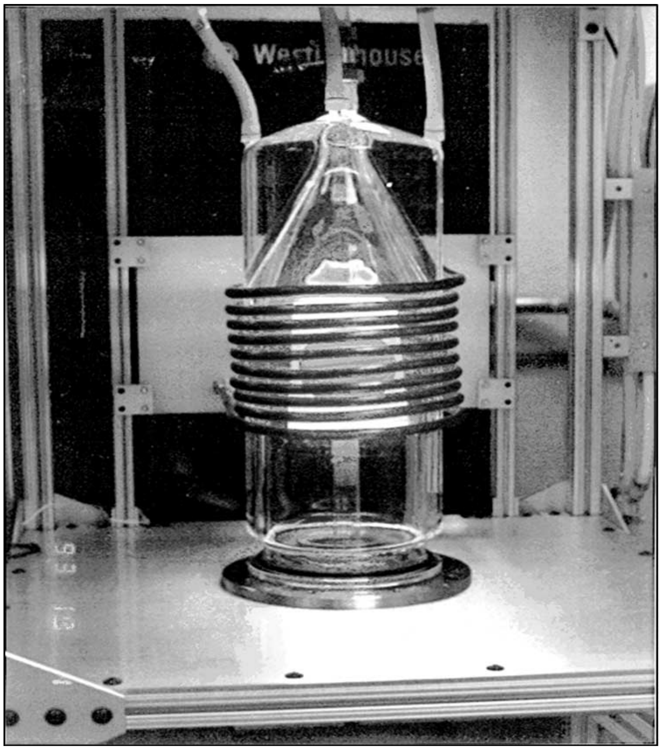

Fig. 3. APCVD SiC Reactor.

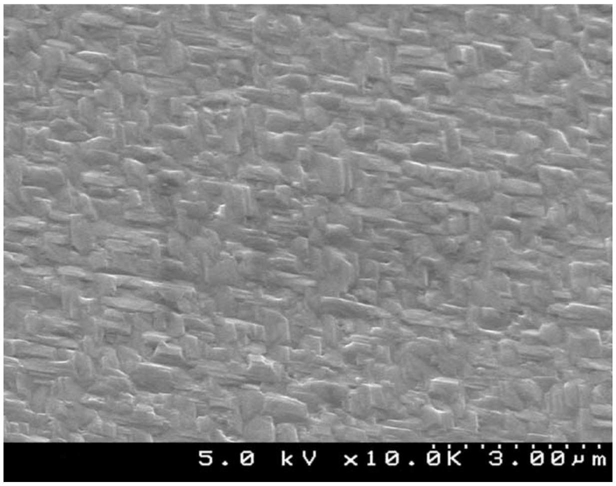

Fig. 4. Plan view SEM micrograph of an as-deposited 3C-SiC surface.

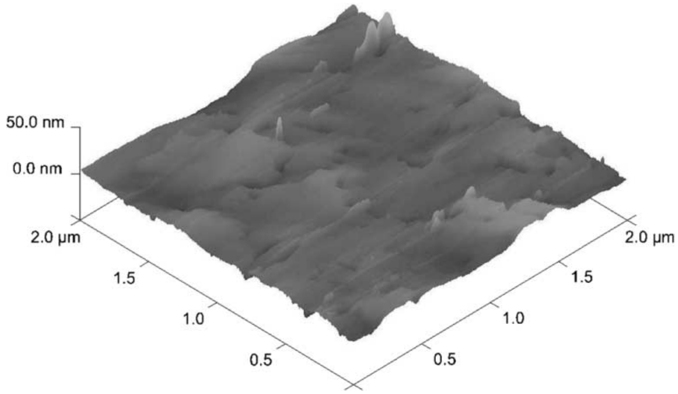

Fig. 5. AFM 3-D profile of a polishing 3C-SiC surface.

diaphragm over a vacuum cavity can be determined using $P_T = (64D/r^4)g + 0.488(64Dg^3/r^4t^2) + 4\sigma(tg/r^2)$, where r and t are the diaphragm radius and thickness, respectively, g is the cavity depth, and D and σ are the diaphragm flexural rigidity and residual stress, respectively. The first term in the equation is due to the diaphragm bending stress, the second and third terms are contributed by the diaphragm stress caused by membrane stretching and residual stress, respectively. If a strong residual tensile stress dominates the compliance of the diaphragm, the touch point pressure can be approximated by the last term, namely $4\sigma(tg/r^2)$. A sensor linear range typically on the order of $\mathrm{P_T}$ can be achieved [2]. Devices satisfying a wide range of performance specifications thus can be fabricated by properly choosing the component geometrical parameters. With a set of masks of fixed lateral dimensions, the same objective can be achieved by adjusting the device vertical dimensions accordingly, an attractive advantage of the proposed sensor architecture. For devices with a partially sealed cavity, the cavity pressure will introduce an offset, thus resulting in an increased touch point pressure.

III. SINGLE-CRYSTAL 3C-SiC THIN FILM

3C-SiC thin films are grown on 100-mm diameter, $\langle 100 \rangle$ silicon wafers in a cold wall, RF-induction heated reactor, as

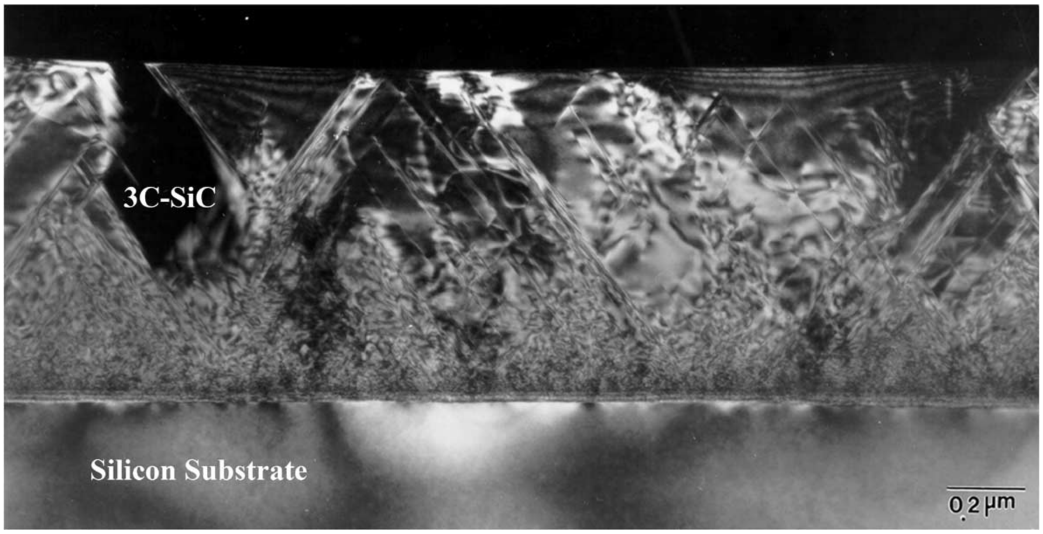

Fig. 6. Cross-sectional TEM micrograph of a 3C-SiC film on a silicon substrate.

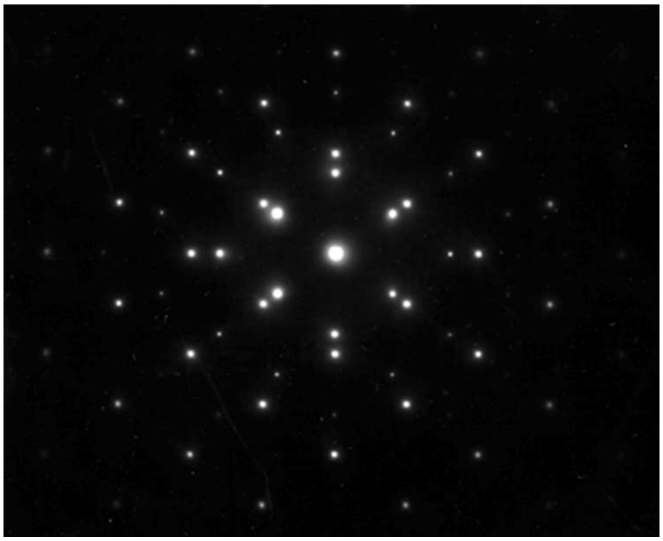

Fig. 7. Selected area electron diffraction pattern of the 3C-SiC/Si interface.

shown in Fig. 3, by atmospheric pressure chemical vapor deposition (APCVD) using a three-step recipe. Details concerning the reactor design and operation can be found elsewhere [10], [11]. SiH_4 (5% in H_2) and C_3H_8 (15% in H_2) are used as Si- and C-containing precursors, and H_2 is used as a carrier gas. A SiC-coated, graphite susceptor is used to hold and heat the wafers. Therefore, a continuous 3C-SiC thin film can be grown only on one side of each wafer. The three-step deposition process begins with an *in-situ* H_2 etch, followed by the formation of a thin 10-nm 3C-SiC layer on the silicon surface by carbonization and continued by bulk 3C-SiC growth. The H_2 etch is performed at 1000 °C and is used to properly prepare the silicon surface for epitaxy by removing the native oxide, as well as any organic contaminants from the substrate surface. After the H_2 etch, the susceptor is cooled to below 500 °C. Carbonization is then initiated by heating the susceptor to 1280 °C in a mixture of C_3H_8 (15% in H_2) and the H_2 carrier gas. The flow rates of C_3H_8 and H_2 are 84 standard cubic centimeters per minute (sccm) and 25 standard liters per minute (slm), respectively. Once reaching the growth temperature, the susceptor temperature and flow rates are held constant for 90 s. After carbonization, 3C-SiC growth is continued by simultaneously reducing the C_3H_8 flow to 26 sccm and introducing SiH_4 (5% in H_2) at 102 sccm into the H_2 carrier gas. Temperature and flow rates are held constant for the duration of the process. Using this procedure, 500 nm-thick 3C-SiC films are grown at a rate of approximately 1000 nm/h. After film growth, the surface is etched in H_2 for 60 s at 1280 °C, after which the wafer is cooled to room temperature in argon and unloaded.

Fig. 4 presents a plan view SEM micrograph of the surface of an as-deposited 3C-SiC film. Despite the fact that the 3C-SiC films exhibit a specular surface appearance when observed optically, the SEM indicates that the surface is textured to the extent that polishing is required to improve the surface quality for wafer bonding. Fig. 5 shows an AFM three-dimensional (3-D) surface profile of a polished surface with an average roughness of 5 nm and a variation of 2 nm.

Fig. 6 presents a cross-sectional TEM micrograph of an as-deposited 3C-SiC, showing both the 3C-SiC film and silicon substrate. The micrograph clearly shows the presence of crystalline defects in the 3C-SiC layer, with the density highest at the film and substrate interface. This micrograph is characteristic of epitaxial 3C-SiC films in that the defect density is highest at the interface as a result of the nearly 20% lattice mismatch between 3C-SiC and silicon. Such a high level of defects has been a recurring problem for 3C-SiC-based piezoresistive pressure sensors since the defects tend to suppress the piezoresistive properties, thus degrading the device sensitivity. For capacitive sensor designs, such as the device reported herein, the high defect density does not impact to the sensor performance because the device capacitance value is independent of the SiC piezoresistive characteristics. Fig. 7 presents a selected area electron diffraction pattern of the 3C-SiC and silicon interface showing that despite the high defect density in the 3C-SiC layer, the film is still epitaxially aligned with the silicon substrate.

The residual stresses in the as-deposited 3C-SiC films grown using the process described above are always tensile and about 200 MPa in magnitude, as determined by wafer curvature

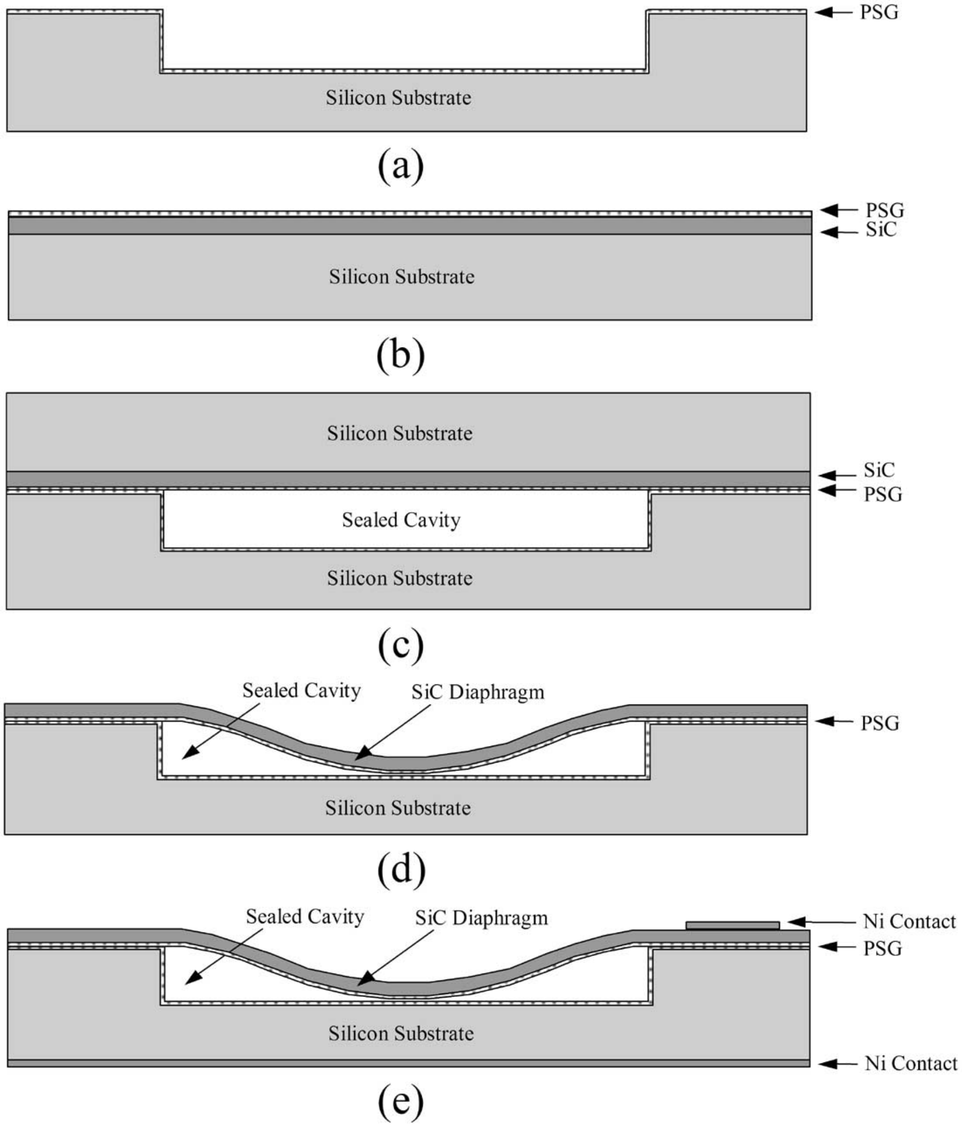

Fig. 8. Sensor fabrication process flow. (a) Recession formation, (b) 3C-SiC Growth and PSG Deposition, (c) wafer bonding, (d) diaphragm formation, and (e) contact metallization.

measurements and confirmed by performing the load-deflection technique on bulk micromachined 3C-SiC membranes [12]. The Young's modulus of the 3C-SiC films is around 360 GPa determined by the load-deflection technique [12]. The load deflection measurements also show the 3C-SiC films to be extremely durable, with 1×1 mm^2 and 0.2-μm-thick membranes able to sustain over 100 psi of differential pressure without bursting, despite the high defect density in the films. This characteristic is critical for realizing sensors that must function over a large pressure range.

IV. CAPACITIVE PRESSURE SENSOR FABRICATION PROCESS

Fig. 8 presents the fabrication process flow for the proposed capacitive pressure sensor. A 4-in N-type $\langle 100 \rangle$ silicon wafer is etched by a reactive ion etch (RIE) process to form a 2-μm recess followed by depositing 2500 Å of phosphorus silicate glass (PSG) as an insulation layer, as shown in Fig. 8(a). Next, a 0.5-μm single-crystal 3C-SiC is grown on the surface of another 4-in N-type $\langle 100 \rangle$ silicon wafer using the APCVD technique described in Section III. The 3C-SiC thin film exhibits a resistivity of approximately 0.5 Ω·cm and a tensile stress of 200 MPa. The SiC surface is then polished by a chemical mechanical polishing (CMP) step to minimize surface roughness and defects. A 2500 Å of PSG film is then deposited on the SiC surface, as shown in Fig. 8(b). This PSG layer covers any remaining surface defects, an important step for success in the subsequent wafer bonding step. The two wafers are annealed at 1000 °C under atmospheric pressure for an hour followed by a minor CMP step to achieve a smooth surface. The wafers are then thoroughly cleaned using a reverse RCA process to obtain hydrophilic surfaces and are bonded together at a pressure of approximately 360 torr, as shown in Fig. 8(c). A high-temperature annealing step at 1000 °C for 2 h is then performed to enhance the bonding quality. In the next step, the silicon substrate above the SiC layer is removed by TMAH to form a 0.5-μm-thick SiC diaphragm. Due to the differential pressure, the diaphragm deflects toward

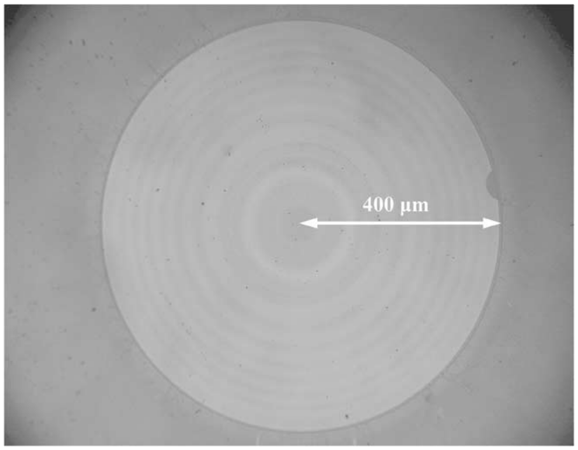

Fig. 9. Top view of a SiC capacitive pressure sensor.

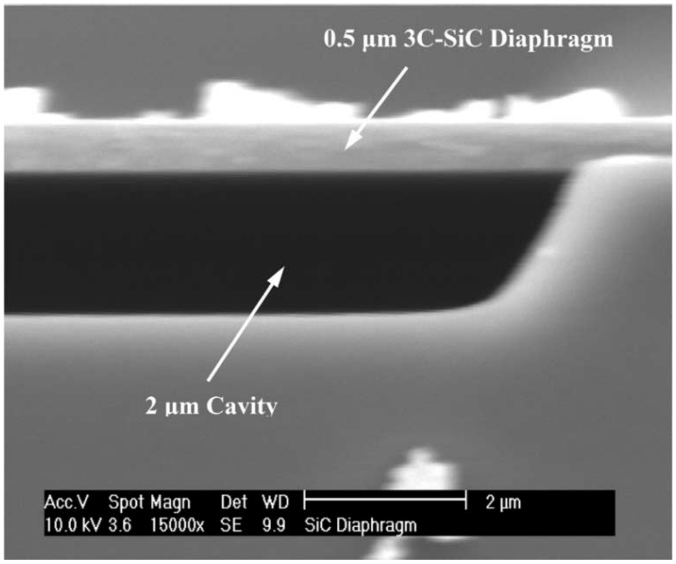

Fig. 10. Cross-sectional SEM of a 3C-SiC-based capacitive pressure sensor.

the substrate and can touch the substrate depending on its structural compliance, as illustrated in Fig. 8(d). A 5000-Å nickel layer is then sputtered on both sides of the wafer using 100 Å of titanium for adhesion enhancement. The nickel film is patterned to form a high-temperature contact to the diaphragm [13], as depicted in Fig. 8(e). The wafer is then diced followed by gold wire bonding and applying high-temperature silver epoxy to establish electrical contacts to the top and bottom electrodes of the sensor, respectively, for device testing.

V. MEASUREMENT RESULTS

Fig. 9 shows a top view optical microscope photo of a fabricated SiC pressure sensor with a 400-μm-radius circular diaphragm. Newton rings are visible, indicating diaphragm bending due to the differential pressure across the diaphragm. Fig. 10 presents a cross-sectional SEM micrograph of the device, illustrating the 0.5-μm SiC layer suspended over a 2-μm recess on the silicon substrate. The SiC diaphragm appears flat due to the equal pressure on both sides of the diaphragm caused by the intentional breaking of the cavity for the SEM. The fabricated sensors are annealed at 400 °C under atmospheric pressure for 48 h to eliminate any device initial temperature dependence and drift prior to characterization. Fig. 11 shows a photo of a general testing setup consisting of a high-temperature testing chamber, external pressure control unit, and temperature and LCR meters. The pressure sensor is attached to a ceramic substrate by high-temperature silver epoxy and gold-wire-bonded to the substrate interconnect pads. The testing module is placed inside a sealed metal testing chamber equipped with a pressure and ceramic-heater-temperature control. A thermal couple is positioned in close proximity to the sensor for measuring the device temperature as shown in Fig. 12. A high-temperature ceramic-based package with precious metal interconnects will be considered for the sensor packaging in the future [14]. The current testing setup is susceptible to parasitic capacitance variations associated with the wiring interconnects. A high-temperature sensing and data telemetry system employing SiC transistors will be attractive for eliminating this undesirable effect. The device capacitance value is measured by a LCR meter as the chamber pressure is varied. The sensor has a nominal capacitance value of approximately 300 pF, dominated by the on-chip parasitic capacitance due to an excessive bonding area in the prototype design. Fig. 13 presents the measured sensor capacitance change versus an externally applied pressure at 200 °C. The device exhibits a touch point pressure of approximately 720 torr with a total capacitance change of 13.5 pF over a

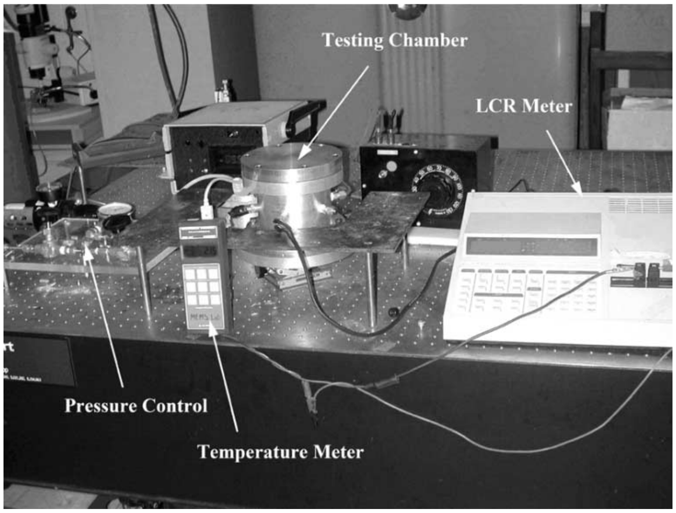

Fig. 11. Testing setup.

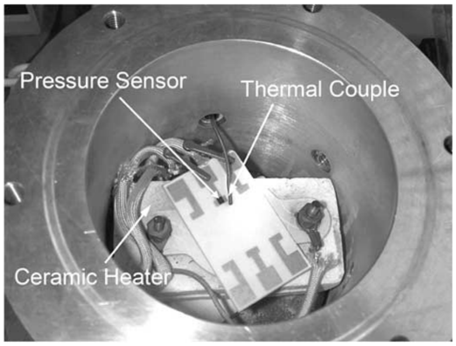

Fig. 12. Pressure sensor testing module.

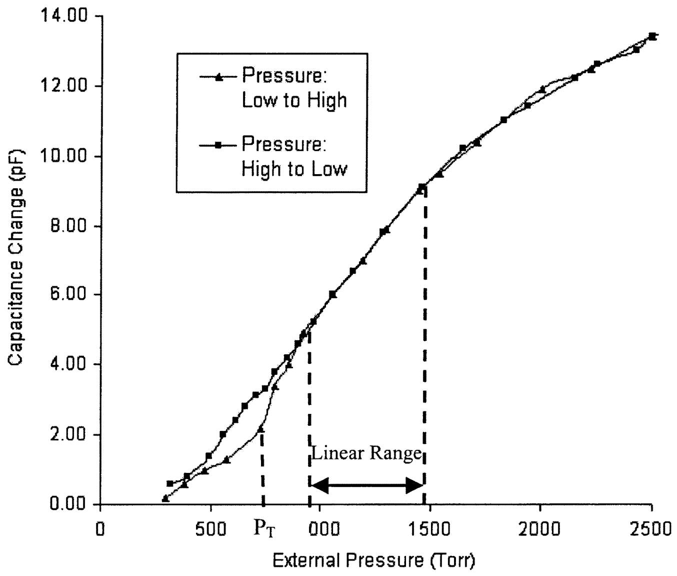

Fig. 13. Sensor characteristic response at 200 °C.

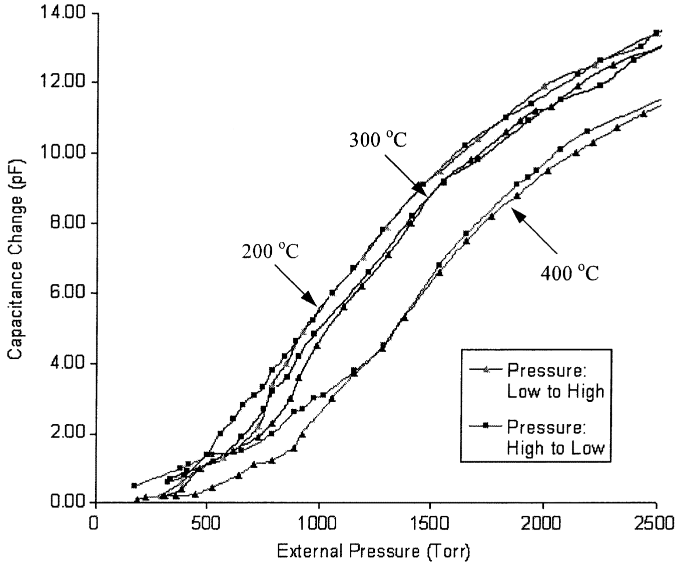

Fig. 14. High-temperature sensor response.

pressure range from 295 to 2500 torr. The sensor achieves a linear characteristic response between 900 and 1450 torr with a sensitivity of 8.0 fF/torr and enters a saturation region with a reduced sensitivity beyond 1500 torr due to the device geometry. Various linear ranges and sensitivities can be obtained by properly choosing the device geometrical parameters. The device exhibits a linearity of 0.7% and a hysterisis of 0.5% within the linear range. The high-temperature sensor performance has been demonstrated up to 400 °C as shown in Fig. 14 and is limited by the current test setup. At 400 °C, the device exhibits an expected touch-mode behavior with a touch point pressure of approximately 1000 torr and achieves a linear characteristic response between 1100 and 1760 torr with a sensitivity of 7.7 fF/torr, a linearity of 2.1%, and a hysterisis of 3.7%. The measurement results indicate that the prototype capacitive pressure sensor is tolerant of contact resistance variations at elevated temperatures. However, the device exhibits separate characteristic curves at different temperatures, as shown in Fig. 14, due to the trapped air inside the cavity. The trapped air causes the sensor touch point pressure to increase near linearly with the temperature, thus resulting in separate characteristic curves. This temperature dependent effect can be substantially minimized by eliminating the trapped air inside the cavity, which can be achieved by wafer bonding in vacuum. However, the thermal expansion coefficient mismatch between the SiC diaphragm and silicon substrate is expected to cause certain temperature dependence for the device. A temperature sensor will thus be required for sensor calibration. The device characteristics measured at the same temperature at different days show a maximum capacitance variation of 0.3 pF within the linear range, thus responding to a sensing repeatability of 39 torr (52 mbar). The demonstrated prototype sensor performance is adequate for various high-temperature sensing applications.

VI. CONCLUSION

SiC is a critical material for sensors operating in high-temperature environments. The proposed capacitive pressure sensors employing single-crystal 3C-SiC diaphragms grown by APCVD technique have demonstrated sensing capabilities up to 400 °C, suitable for various high-temperature applications. The fabricated devices are tolerant of high-temperature contact resistance variations. The exhibited device temperature dependence can be substantially minimized by wafer bonding in vacuum.

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