

Single Crystal SiC MEMS Fabrication Technology Using Smart-Cut Process for Harsh Environment Application

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Abstract

A new single crystal silicon carbide MEMS fabrication process is developed using proton-implantation smart-cut technique. A 6H-SiC layer with 1.3 μm thickness has been achieved over an oxidized silicon substrate using the proposed technique. TEM analyses of the silicon carbide thin film reveal single crystal characteristics, which is attractive for potential integration of MEMS devices with high-temperature microelectronics in the same structural layer for harsh environment applications. Implant-induced defect density in the silicon carbide can be substantially reduced to a negligible level through high-temperature annealing. Prototype single crystal 6H-SiC MEMS devices, such as resonators and actuators, have been successfully fabricated as demonstration vehicles for future harsh-environment micro-system implementation.

Keywords

MicroElectroMechanical Systems (MEMS), Single Crystal Silicon Carbide Device, Harsh-Environment Application, High-Temperature Sensors and Actuators

INTRODUCTION

Single crystal silicon carbide (SiC) material is highly critical for implementing MicroElectroMechanical Systems (MEMS) for high-temperature applications due to its mechanical robustness, chemical inertness, and electrical stability at elevated temperatures [1, 2]. Most MEMS devices require a structural layer over an oxide sacrificial material. Such structures based on SiC have been demonstrated by using single crystal 3C-SiC films, which can be hetero-epitaxially grown on silicon substrates, and wafer bonding techniques to fabricate MEMS sensors for harsh environment applications [3, 4]. However, the 3C-SiC material exhibits a large amount of defects, which is inadequate for building high-performance microelectronic devices, thus hindering potential system integration [5]. In this paper, a new single crystal 6H-SiC MEMS fabrication technology based on proton-implantation smart-cut process is presented. 6H-SiC material is widely used for high-performance microelectronics. Similar techniques have been proposed to produce low-cost silicon on insulator wafers for low-power microelectronics and MEMS applications [6, 7, 8]. At present most MEMS devices call for a structural layer with a thickness of at least 1 μm to achieve desired performance. In this research a single crystal 6H-

SiC layer with a thickness of 1.3 μm is demonstrated for MEMS applications. TEM analyses of the resulting SiC layer reveal a negligible implant-induced defect density due to high-temperature annealing and single crystal material characteristics, which are highly desirable for potential integration of MEMS devices with high-temperature sensing and control electronics in the same structural layer for building high-performance harsh-environment micro-systems. Furthermore, the silicon carbide film thickness can be accurately determined through an implant energy control, which presents a key advantage for high-precision device fabrication. The proposed technique allows an original single crystal 6H-SiC substrate to be reused for the fabrication process, thus potentially resulting in a significant substrate and processing cost reduction. SiC MEMS prototype devices, such as resonators and actuators with a typical device dimension of a few hundreds of micrometers and a final thickness of 1.2 μm , have been fabricated as demonstrated vehicles for future high-temperature sensors, actuators, and micro-systems implementation. A thicker SiC layer can be obtained by enhancing the implant energy but will be ultimately limited by the equipment capability.

FABRICATION PROCESS

The proposed single crystal SiC MEMS fabrication process flow is presented in Figure 1. The process begins with a commercial 2-inch N-type 6H-SiC wafer from Cree, Inc. The wafer exhibits a thickness of 260 μm with a resistivity of 0.05 $\Omega\cdot\text{cm}$ and is passivated by a 1000 \AA of thermal oxide, which serves as a surface protection layer for wafer handling during the subsequent implant. A proton dosage of $1 \times 10^{17}/\text{cm}^2$ has been shown adequate for silicon carbide layer splitting [9] and thus is selected for this experiment. The proton peak concentration location can be controlled by the implant energy. An implant energy of 200 KeV is chosen to achieve an expected H^+ peak concentration of approximately 1.3 μm below the wafer surface, as illustrated in Figure 1a, based on an implant projected range calculation of approximately 65 nm/KeV in silicon carbide. The implanted hydrogen ions introduce micro-cavities along the peak concentration. After bonded to a carrier substrate, the micro-cavities will cause the silicon carbide wafer to split along the peak concentration by a high-temperature annealing step [9], thus resulting in a single crystal 6H-SiC layer with a thickness of about 1.3 μm over the carrier substrate. This silicon carbide layer

thus can be used as a structural material for building high-temperature MEMS sensors and actuators. The silicon carbide thickness can be increased by enhancing the implant energy but is ultimately limited by the equipment capability and processing time. Conventional medium-current implant equipment employed for achieving the required dose range is typically limited to a maximum implant energy of around 400 KeV, corresponding to a thickness of approximately 2.6 μm . Low-current implant equipment can offer higher implant energy but making the processing time and cost prohibitive.

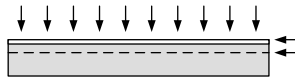


Figure 1a. Proton Implantation



Figure 1b. Oxidizing Silicon Carrier Wafer

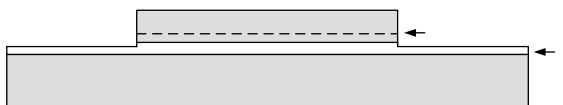


Figure 1c. Wafer Bonding

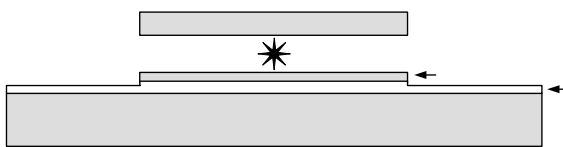


Figure 1d. SiC Wafer Splitting



Figure 1e. Aluminum Deposition and Patterning



Figure 1f. Split SiC Layer Etching



Figure 1g. Released Microstructure

Figure 1. Single Crystal Silicon Carbide MEMS Process

In next step, a 4-inch $\langle 100 \rangle$ N-type silicon substrate, serving as a carrier wafer, is passivated by a thermal oxide. An

oxide thickness of 2 μm is chosen for the prototype fabrication as shown in Figure 1b. After a minor polishing of both wafers surface, the two substrates are extensively cleaned in DI water followed by a reverse RCA cleaning to remove any particles and ionic contaminations and also to obtain hydrophilic surfaces. The two substrates are then brought into contact and initially bonded together at room temperature, followed by an annealing at 300 $^{\circ}\text{C}$ for 24 hours to maximize the bonding strength as shown in Figure 1c. The bonded wafers are then heated at 1000 $^{\circ}\text{C}$ for 8 hours to initiate the splitting, causing an approximately 1.3 μm -thick single crystal 6H-SiC layer transferred from the SiC wafer to the silicon substrate, as depicted in Figure 1d. The splitting condition is experimentally determined for the prototype fabrication as a lower temperature process would require an excessive annealing time to initiate the splitting, while a higher temperature annealing may separate the wafers from the bonding interface if the initial bonding is weak. Furthermore, a slow temperature ramping over one hour is applied to avoid an excessive thermal shock that could also potentially separate the wafers at the oxide interface. After the splitting, the 6H-SiC wafer can be polished and reused by the same procedure to form SiC on insulator (SiCOI) substrates, thus substantially reducing the substrate fabrication cost. At this point, the SiCOI wafer is annealed at 1150 $^{\circ}\text{C}$ for over 4 hours. This annealing step not only forms a strong chemical bond at the oxide interface but also substantially reduces the implant-induced defects in the transferred SiC layer to a negligible level. An aluminum layer with a thickness of 1000 \AA is then sputtered on the SiC surface and patterned to form an etch mask as shown in Figure 1e. The SiC layer is etched using a reactive ion etch employing O_2 , CHF_3 , and He_2 as etch gases with an etch rate of approximately 250 $\text{\AA}/\text{min}$. The aluminum layer is then removed with a wet etch as shown in Figure 1f. At this point the wafer is coated by a 1.5 μm -thick photoresist as a protection layer for wafer dicing. After dicing, the photoresist layer is removed followed by releasing MEMS devices in a timed HF etch as depicted in Figure 1g.

Proton Implantation

SiC Wafer

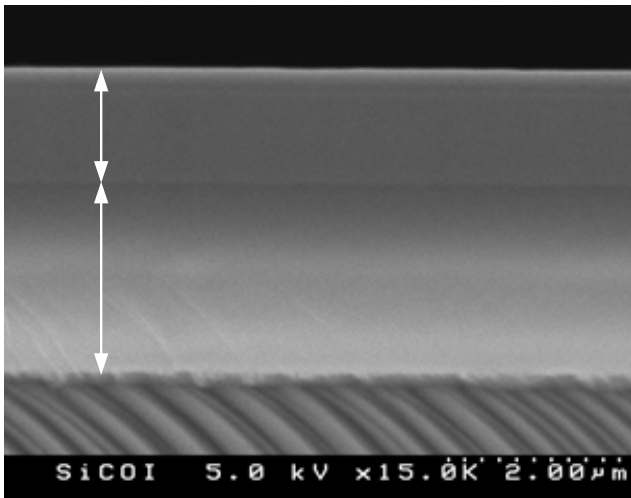


Figure 2. Wafer Cross-Sectional View After Splitting

FABRICATION AND MEASUREMENT RESULTS

Figure 2 presents an SEM photo of the wafer cross-section after the splitting, showing that a $1.3\ \mu\text{m}$ -thick silicon carbide layer is transferred onto the silicon carrier substrate passivated by a $2.2\ \mu\text{m}$ -thick thermal oxide. The obtained silicon carbide layer achieves a uniform thickness with a variation of $100\ \text{\AA}$ and a smooth surface. The surface quality is characterized by an atomic force microscope (AFM). Figure 3 presents an AFM three-dimensional surface profile with an average roughness of $4.6\ \text{nm}$. The small surface roughness can be further improved by a minor polishing step to obtain a high quality surface.

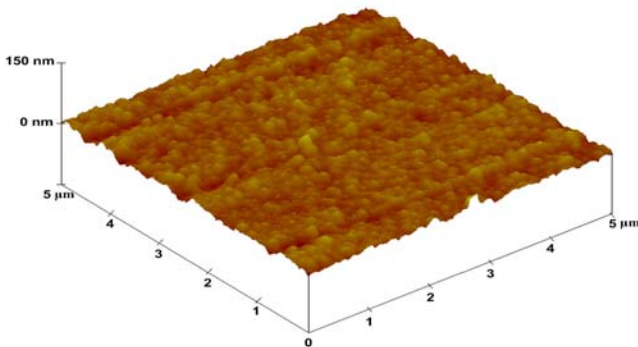


Figure 3. AFM Three-Dimensional Surface Profile

TEM analyses have been performed to analyze the silicon carbide material characteristics. Figure 4 presents a dark field TEM cross-section image of the split SiC layer after the annealing, showing a final SiC layer thickness of $1.2\ \mu\text{m}$ with a $0.2\ \mu\text{m}$ of surface oxide caused by oxidation. The surface oxidation can be avoided in the future if the high-temperature splitting and annealing processes are conducted in a non-oxygen environment. The TEM of the SiC region exhibits a negligible defect density and is indistinguishable from that of the original single crystal 6H-SiC substrate. Figure 5 shows a selected area Electron Diffrac-

tion Pattern (SAD) of the split silicon carbide material. The diffraction pattern indicates single crystal characteristics, which is critical for realizing high-performance MEMS devices and potential system integration with high-temperature microelectronics in the same structural layer for harsh environment applications.

A number of prototype microstructures such as resonators and actuators have been successfully fabricated using the proposed fabrication technology. Figure 6a presents an SEM photo of a fabricated 6H-SiC micro-resonator. The device exhibits a length of $450\ \mu\text{m}$ with a beam width of $4.5\ \mu\text{m}$, comb finger spacing of $2.5\ \mu\text{m}$, and structural thickness of $1.2\ \mu\text{m}$. A close view of the comb fingers and proof mass are shown in Figure 6b. The resonator is freely released from the substrate with an underneath $2.2\ \mu\text{m}$ of air gap. The demonstrated MEMS structures can be used as building blocks to design and fabricate more complex micro-systems for harsh environment applications in the future.

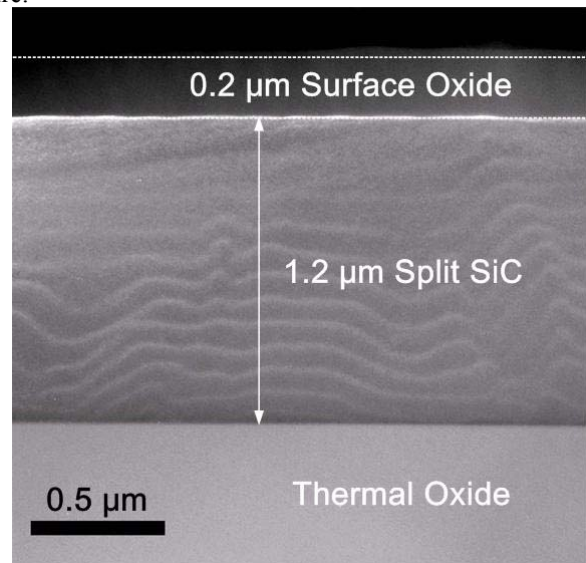


Figure 4. TEM of Annealed Split SiC Cross Section

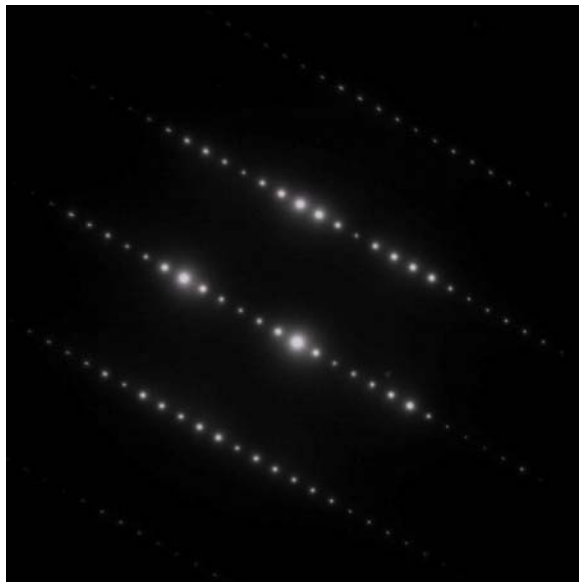


Figure 5. SAD of the Split SiC Layer

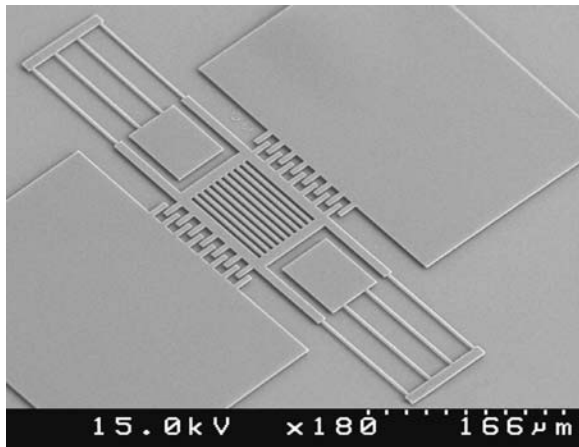


Figure 6a. Fabricated 6H-SiC Resonator Top View

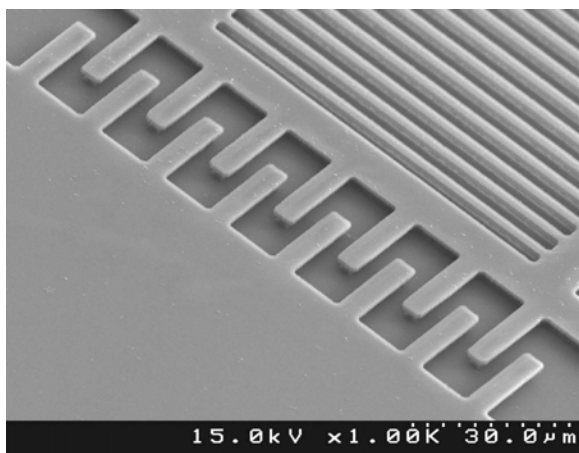


Figure 6b. Resonator Comb Fingers and Proof Mass

CONCLUSION

A single crystal 6H-SiC MEMS fabrication technology has been demonstrated using proton-implantation smart-cut technique. Prototype MEMS resonators and actuators have been successfully fabricated as demonstration vehicles for future high-performance harsh-environment micro-system implementation. The proposed technique allows an original single crystal 6H-SiC substrate to be reused for the fabrication process, thus potentially resulting in a significant substrate and processing cost reduction. Material analyses show that the transferred silicon carbide layer reveals single crystal characteristics and exhibits a negligible defect density after high-temperature annealing. These characteristics are critical for realizing high-performance MEMS sensors, actuators, and potential system integration with high-temperature microelectronics in the same structural layer. The proposed technology is also attractive for potentially realizing other single crystal thin films, such as GaAs and GaN, on an insulated carrier substrate for integrating micro-systems with optoelectronics.

ACKNOWLEDGMENT

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REFERENCES

- [1] M. Mehregany, C. A. Zorman, N. Rajan, C. H. Wu, "Silicon Carbide MEMS for Harsh Environments," *Proceeding of the IEEE*, Vol. 86, No. 8, pp. 1594-1610, 1998.
- [2] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High temperature electronics – A role for wide bandgap semiconductors?" *Proceedings of the IEEE*, vol. 90, June 2002, pp. 1065-1076.
- [3] C. H. Wu, S. Stefanescu, H. I. Kuo, C. A. Zorman, and M. Mehregany, "Fabrication and Testing of Single Crystal 3C-SiC Piezoresistive Pressure Sensors," *Technical Digest, International Conference on Solid-State Sensors and Actuators*, pp. 514-517, 2001.
- [4] D. J. Young, J. Du, C. A. Zorman, W. H. Ko, "High-Temperature Single Crystal 3C-SiC Capacitive Pressure Sensor," *IEEE Sensors Journal, Special Issue on Microsensors and Microactuators*, August 2004, pp. 464-470.
- [5] P. G. Neudeck, D. J. Larkin, J. E. Starr, J. A. Powell, C. S. Salupo, and L. G. Matus, "Greatly Improved 3C-SiC p-n Junction Diodes Grown by Chemical Vapor Deposition," *IEEE Electron Device Letters*, vol. 14, issue 3, pp. 136-139, 1993.
- [6] A. J. Auberton-Herve, M. Bruel, B. Aspar, C. Maleville, and H. Moriceau, "Smart-cut: The Basic Fabrication Process for UNIBOND SOI Wafers," *IEICE Trans. Electron.*, Vol. E80-C, pp. 358-363, 1997.

- [7] J. Du, W. H. Ko, D. J. Young, "Single Crystal Silicon MEMS Fabrication Based On Smart-Cut Technique," *Sensors and Actuators*, vol. 112, issue 1, pp. 116-121, 2004.
- [8] C-H Yun and N. W. Cheung, "Fabrication of Silicon and Oxide Membranes Over Cavities Using Ion-Cut Layer Transfer," *IEEE Journal of Microelectromechanical Systems*, Vol. 9, No. 4, pp. 474-477, December 2000.
- [9] Q.-Y. Tong, K. Gutjahr, S. Hopfe, U. Gösele, and T.-H. Lee, "Layer splitting process in hydrogen-implanted Si, Ge, SiC, and diamond substrates," *Applied Physics Letters*, Vol. 70(11), pp. 1390-1392, March 1997.