Available online at www.sciencedirect.com

SCIENCE DIRECT®

Sensors and Actuators A 112 (2004) 116–121

SENSORS AND ACTUATORS A PHYSICAL

www.elsevier.com/locate/sna

Single crystal silicon MEMS fabrication based on smart-cut technique

Jiangang Du, Wen H. Ko, Darrin J. Young*

EECS Department, Case Western Reserve University, 10900 Euclid Avenue, Cleveland, OH 44106-7221, USA

Received 23 July 2003; received in revised form 24 November 2003; accepted 29 November 2003

Abstract

A new single crystal silicon MicroElectroMechanical Systems (MEMS) fabrication process is proposed using proton-implantation smart-cut technique. Compared to conventional silicon on insulator (SOI) wafer fabrication processes for MEMS applications, this technology can potentially result in a significant substrate and processing cost reduction. A silicon layer with 1.79 μm thickness has been achieved over an oxidized 4-in silicon substrate using the proposed technique. TEM analyses of the silicon thin film reveal single crystal characteristics, which is attractive for potential integration of MEMS devices with microelectronics in the same structural layer. Implant-induced defect density in the silicon can be substantially reduced to a negligible level through high temperature annealing. Prototype single crystal silicon MEMS structures, such as cantilever beams and clamped–clamped micro-bridges with a typical length of a few hundreds of micrometers, have been successfully fabricated as demonstration vehicles for future micro-systems implementation.

Keywords: MEMS fabrication; Single crystal silicon MEMS; Smart-cut; Ion-implant

1. Introduction

Single crystal silicon material is highly desirable for implementing MicroElectroMechanical devices and systems due to its reliable and reproducible mechanical and electrical properties [1]. Silicon on insulator (SOI) wafers have been used to realize single crystal silicon MEMS inertial sensors, optical devices, field emission components, etc. [2–5]. The silicon structural layer is typically obtained through wafer bonding followed by a grinding and chemical mechanical polishing (CMP) step [3,6]. This technique, however, results in a substantial amount of silicon material loss through the grinding and CMP processes; hence increasing the substrate and processing cost. In this paper, a new single crystal silicon MEMS fabrication technology based on proton-implantation smart-cut technique is presented. This technique has been proposed to produce low cost SOI wafers, with a typical silicon thickness on the order of a hundred nanometers, for low power microelectronics applications [7,8]. A similar technique has been employed to demonstrate suspended thin silicon membranes with a comparable thickness over recess cavities for potential MEMS applications [9]. At present, most MEMS devices call for silicon structural layer with a thickness of at least 1 μm, sometimes a few tens of micrometers, to achieve the desired performance. In this research a single crystal silicon layer with a thickness close to 2 μm is demonstrated by increasing the proton implant energy for MEMS applications. TEM analyses of the resulting silicon layer reveal a negligible implant-induced defect density due to high temperature annealing and single crystal material characteristics, which are highly desirable for potential integration of MEMS devices with sensing and control electronics in the same structural layer for building high-performance micro-systems. Furthermore, the silicon film thickness can be accurately determined through an implant energy control, which presents a key advantage for high-precision devices fabrication. The proposed technique eliminates the grinding and CMP processes required in conventional MEMS SOI wafer preparation, potentially resulting in a significant substrate and processing cost reduction. MEMS prototype structures, such as cantilever beams and clamped–clamped micro-bridges with a typical length of a few hundreds of micrometers and a thickness of 1.7 μm, have been fabricated as demonstrated vehicles for future sensors, actuators, and micro-systems implementation. A thicker silicon layer can be obtained by enhancing the implant energy but will be ultimately limited by the equipment capability. An additional epitaxial growth on top of the existing silicon layer can be potentially considered to increase the layer thickness [10].

---

* Corresponding author. Tel.: +1-216-368-8945; fax: +1-216-368-6039.
E-mail address: djy@po.cwru.edu (D.J. Young).

0924-4247/$ – see front matter © 2003 Elsevier B.V. All rights reserved.
doi:10.1016/j.sna.2003.11.027

2. Fabrication process

The proposed single crystal silicon MEMS fabrication process flow is presented in Fig. 1. A 4-in ⟨1 0 0⟩ N-type prime grade silicon substrate (Wafer A) is first passivated with 1000 Å thermal oxide, which serves as a surface protection layer for wafer handling during the subsequent implant. A proton dosage ranging from 3×10^{16} to $1 \times 10^{17}\,\mathrm{cm}^2$ has been shown to be adequate for silicon layer splitting [11]. An implant dose of $7 \times 10^{16}\,\mathrm{cm}^2$ is thus selected for this experiment to ensure enough buried protons for a successful splitting. An implant energy of 200 keV is chosen to achieve an expected H^+ peak concentration of approximately 1.8 μm below the wafer surface, as illustrated in Fig. 1a, based on an implant projected range calculation of approximately 90 nm/keV in silicon [11]. The implanted hydrogen ions introduce micro-cavities along the peak concentration. After bonded to a carrier substrate, the micro-cavities will cause the silicon wafer to split along the peak concentration by a high temperature annealing step [7,8], thus resulting in a single crystal silicon layer with a thickness of about 1.8 μm over the carrier substrate. This silicon layer thus can be used as a structural material for building MEMS sensors and actuators. The silicon thickness can be increased by enhancing the implant energy but is ultimately limited by the equipment capability and processing time. Conventional medium-current implant equipment employed for achieving the required dose range is typically limited to a maximum implant energy of around 400 keV, corresponding to a thickness of 3.6 μm. Low-current implant equipment can offer higher implant energy but making the processing time and cost prohibitive. A thicker silicon layer, however, can be potentially obtained through an additional epitaxial growth on top of the existing layer. After the implant the oxide passivation layer is removed by HF to obtain a smooth wafer surface, which is critical for the subsequent wafer bonding. In the next step, another 4-in ⟨1 0 0⟩ N-type silicon substrate (Wafer B) serving as a carrier wafer is passivated by a thermal oxide. An oxide thickness of 1.5 μm is chosen for the prototype fabrication as shown in Fig. 1b. After a minor polishing of the oxide surface, Wafer A and Wafer B are cleaned in a base solution ($H_2O:NH_4OH:H_2O_2 = 5:1:1$) to obtain a hydrophilic wafer surface followed by a further cleaning in a standard RCA to remove any possible ionic contaminations. At the point, the as-cleaned wafers are rinsed in DI wafer for an extensive period of time to keep the surfaces free of particles while maintaining hydrophilicity. The two substrates are then brought into contact and bonded together by a compression bonding technique with an in situ infrared-based heating to dispel any trapped water vapor drops, as shown in Fig. 1c. The bonded wafers are annealed at 270 °C for 12 h to enhance the initial bonding strength followed by heating at 485 °C for 30 min to initiate the splitting, causing an approximately 1.8 μm-thick single crystal silicon layer transferred from wafer A to wafer B, as depicted in Fig. 1d. The splitting condition is experimentally determined for the prototype fabrication since a lower temperature process would require an excessive annealing time to initiate the splitting, while a higher temperature annealing may separate the wafers from the bonding interface if the initial bonding is weak. After the splitting, Wafer A can be polished and reused by the same procedure to form SOI substrates, thus eliminating silicon material loss occurring in conventional MEMS SOI wafer preparation, potentially reducing substrate cost. The split silicon layer is then annealed at 1100 °C for over 2 h. This annealing step not

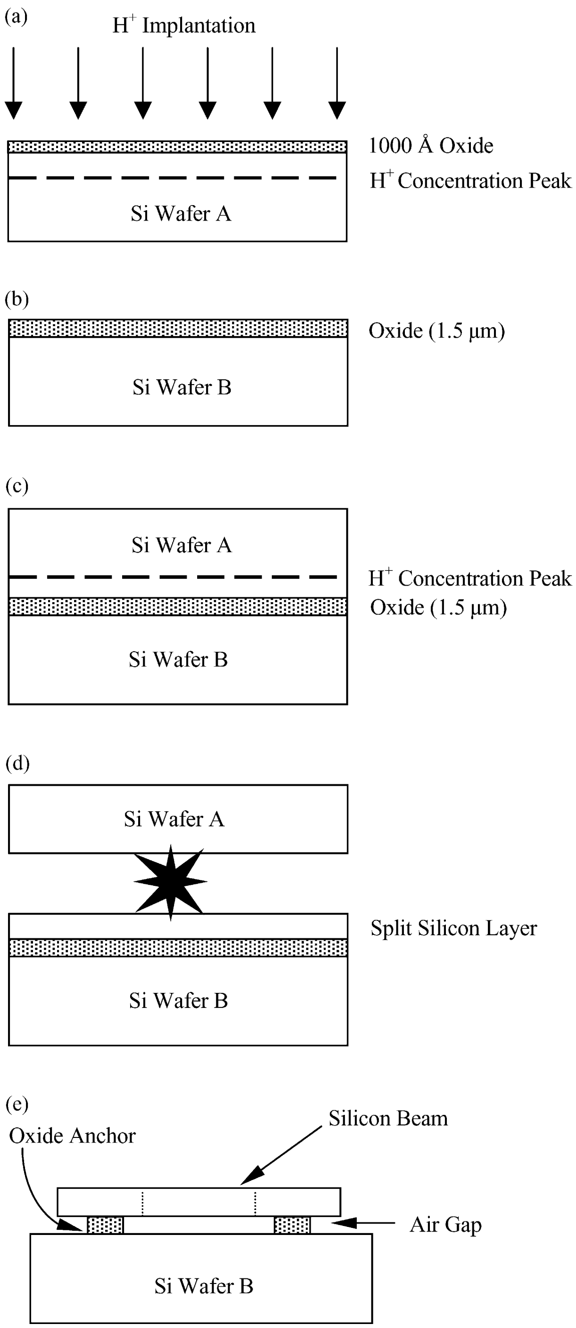


Fig. 1. Single crystal silicon MEMS process flow: (a) hydrogen implantation; (b) oxidizing carrier wafer; (c) wafer bonding; (d) wafer splitting; (e) released microstructure.

only forms a strong chemical bond between the silicon and underneath thermal oxide but also substantially reduces the implant-induced defects in the transferred layer to a negligible level, as will be illustrated in the following section. The split silicon layer is patterned with a standard lithography process and dry etched to form various microstructures, such as cantilever beams and clamped–clamped micro-bridges. The wafer is then diced followed by a timed etch in HF and a super critical drying process to release the microstructures as shown in Fig. 1e.

3. Fabrication and measurement results

Fig. 2 presents an SEM photo of the wafer cross-section after the splitting, showing that a 1.79 μm-thick silicon layer is transferred onto the carrier wafer passivated by a 1.5 μm-thick thermal oxide. The obtained silicon layer achieves a uniform thickness with a variation of 100 Å and a smooth surface. The surface quality is characterized by an atomic force microscope (AFM). Fig. 3 presents an AFM three-dimensional surface profile with an average roughness of 10 nm. The small surface roughness can be readily eliminated by a minor polishing step to obtain a high quality surface and is attractive for high-performance micro-system applications, such as low loss optical communications and biomedical imaging detections.

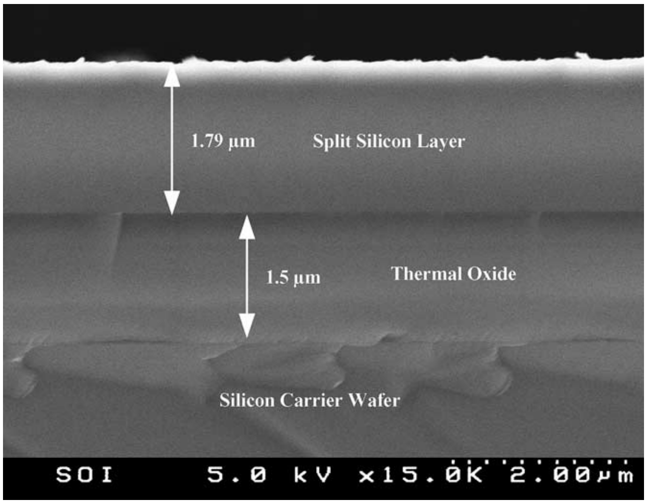


Fig. 2. Wafer cross-sectional view after splitting.

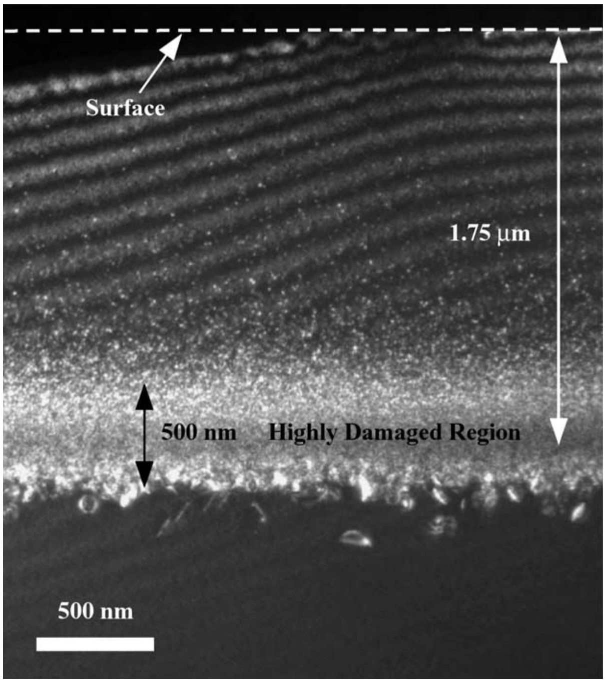


Fig. 4. Dark field TEM of as-implanted silicon cross-section.

TEM analyses have been performed to analyze the silicon material characteristics before and after the splitting. Fig. 4 shows a dark field TEM cross-sectional image of an as-implanted silicon wafer along the ⟨0 1 1⟩ orientation. From the figure, it can be seen that an implant-induced highly damaged silicon layer with a width of 500 nm is located approximately 1.75 μm below the wafer surface. This

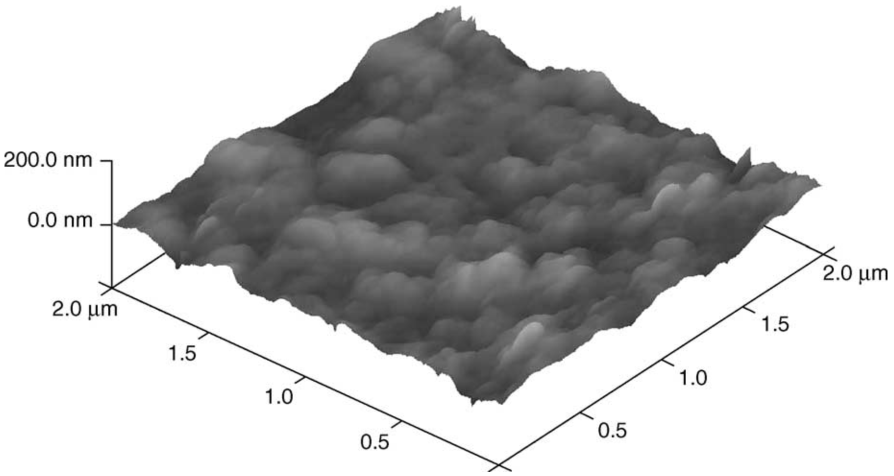


Fig. 3. AFM three-dimensional surface profile.

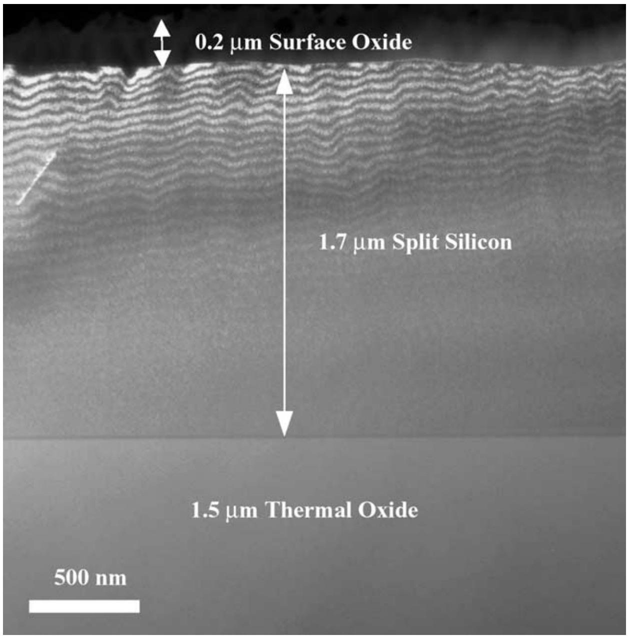


Fig. 5. Dark field TEM of annealed split silicon cross-section.

damaged layer causes the wafer to split when annealed at elevated temperatures. The implant-induced defect density decreases toward the silicon surface and is estimated as 2×10^{11}, 8×10^{10}, and $3 \times 10^{10}\ \mathrm{cm}^{-2}$ at 1.2, 1, and 0.8 μm away from the surface, respectively. The defect density can be significantly reduced by the 1100 °C annealing step after the silicon splitting. Fig. 5 presents a corresponding dark field TEM cross-sectional image of an annealed split silicon layer. Compared to Fig. 4, the defect density in silicon is reduced to a negligible level. An X-ray analysis indicates that a thin oxide layer with a thickness of 0.2 μm is formed at the wafer surface caused by the high temperature annealing in an oxygen environment, thus resulting in a final thickness of 1.7 μm for the split silicon layer. Fig. 6 shows a close view of the interface between the surface oxide and split silicon layer. A thin residual layer of defects with a thickness of 10 nm is found under the surface oxide. However, the TEM of the silicon region underneath is indistinquishable from that of single crystal silicon substrates used for microelectronics fabrication. The surface oxide can be removed by HF followed by a minor CMP process to eliminate the residual defect region to obtain high quality silicon. The high temperature annealing can also be performed in a non-oxygen environment to avoid surface oxidation. However, a CMP step may still be necessary to eliminate any residual defect layer at the split surface. Fig. 7 presents a selected area electron diffraction pattern (SAD) of the split silicon material. The diffraction pattern indicates single crystal characteristics, which is critical for realizing high-performance MEMS devices and potential system integration with microelectronics in the same structural layer.

A number of prototype microstructures have been successfully fabricated using the proposed fabrication technology.

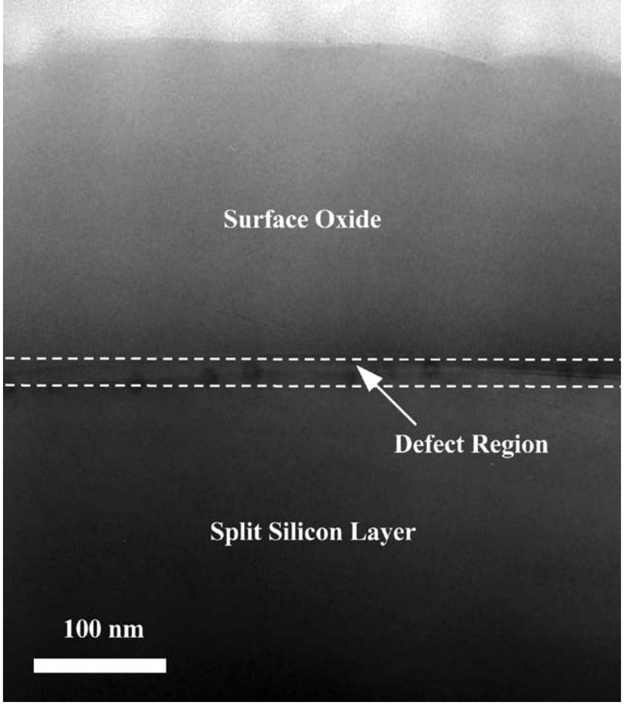


Fig. 6. Close view of the interface between oxide and silicon.

Fig. 8a and b present SEM photos of fabricated cantilever beams and clamped–clamped micro-bridges. These microstructures exhibit a width of 5 μm and lengths ranging from 100 to 190 μm. The structures have a thickness of 1.7 μm since the surface oxide is removed along with

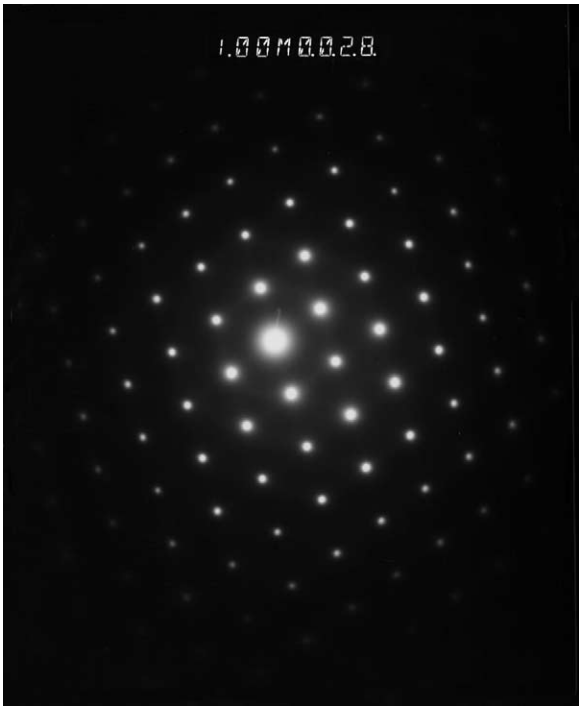
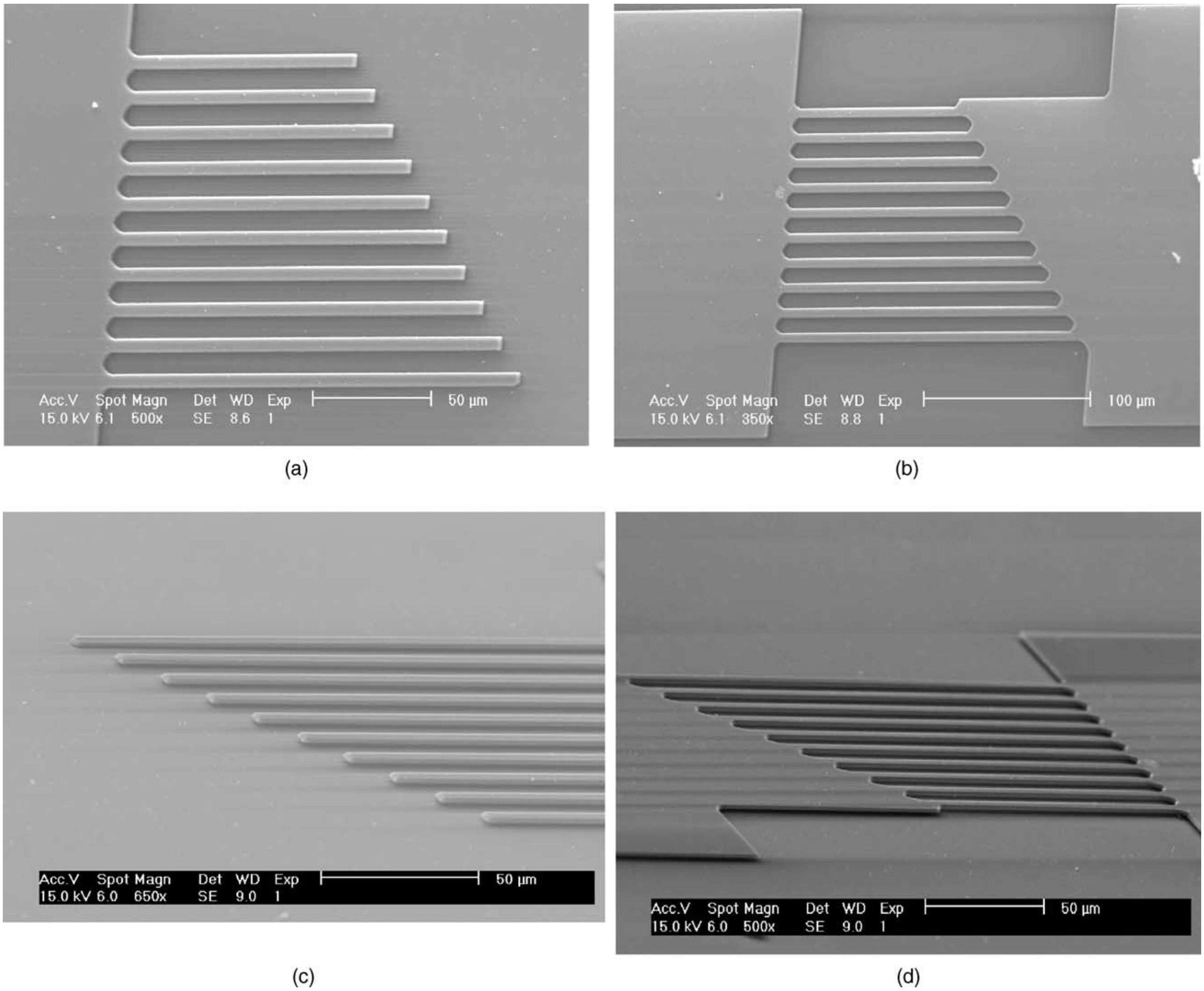


Fig. 7. SAD of the split silicon layer.



(a) (b) (c) (d)

Fig. 8. (a) Fabricated cantilever beams top view. (b) Fabricated clamped–clamped beams top view. (c) Cantilever beams cross-sectional view. (d) Micro-bridges cross-sectional view.

the sacrificial layer during the release. The corresponding cross-sectional views of the structures are shown in Fig. 8c and d, indicating that the beams are freely released and the cantilevers are virtually free of warpage, which is critical for various MEMS applications. These demonstrated structures can be used as building blocks to design and fabricate more complex MEMS sensors and actuators in the future.

4. Conclusions

A single crystal silicon MEMS fabrication technology has been demonstrated using proton-implantation smart-cut technique. The proposed technology, compared to conventional SOI wafer fabrication processes for MEMS applications, can potentially result in a significant substrate and processing cost reduction. Prototype cantilever beams and clamped–clamped micro-bridges have been successfully fabricated as demonstration vehicles for future micro-system implementations. Material analyses show that the transferred silicon layer reveals single crystal characteristics and exhibits a negligible defect density after high temperature annealing. These characteristics are critical for realizing high-performance MEMS sensors, actuators, and potential system integration with microelectronics in the same structural layer. The proposed technology is also attractive for potentially realizing other single crystal thin films, such as SiC, GaAs, and GaN, for implementing micro-systems and electronic devices for harsh environment applications and integration with optoelectronics.

Acknowledgements

This work is partially supported by NASA under Glennan Micro-System Initiative. The fabrication process was performed at Micro-Fabrication Laboratory at Case Western Reserve University.

References

[1] K. Petersen, Silicon as a mechanical material, Proc. IEEE 70 (5) (1982) 420–457.

[2] T. Brosnihan, J.M. Bustillo, A.P. Pisano, R.T. Howe, Embedded interconnect and electrical isolation for high-aspect-ratio, SOI inertial instruments, in: Proceedings of the 1997 International Conference on Solid-State Sensor and Actuators, June 1997, pp. 637–640.

[3] R.A. Conant, J.T. Nee, K.Y. Lau, R.S. Muller, A flat high-frequency scanning micromirror, in: Proceedings of Solid-State Sensor and Actuator Workshop, June 2000, pp. 6–9.

[4] V. Milanovic, M. Last, K.S.J. Pister, Monolithic silicon micromirrors with large scanning angle, in: Proceedings of Optical MEMS 2001, Okinawa, Japan, September 2001, pp. 135–136.

[5] V. Milanovic, L. Doherty, D. Teasdale, S. Parsa, C. Zhang, K.J.S. Pister, Micromachining technology for lateral field emission devices, IEEE Transaction on Electron Devices—special issue on vacuum electronics 48 (1) (2001) 166–173.

[6] L. Parameswaran, C. Hsu, M.A. Schmidt, A merged MEMS-CMOS process using silicon wafer bonding, IEDM, 1995, pp. 613–616.

[7] A.J. Auberton-Herve, M. Bruel, B. Aspar, C. Maleville, H. Moriceau, Smart-cut: the basic fabrication process for UNIBOND SOI wafers, IEICE Trans. Electron. E80-C (1997) 358–363.

[8] Q.-Y. Tong, K. Gutijahr, S. Hopfe, T.-H. Lee, Layer splitting process in hydrogen-implanted Si, Ge, SiC, and diamond substrates, Appl. Phys. Lett. 70 (1997) 1390–1392.

[9] C.-H. Yun, N.W. Cheung, Fabrication of silicon and oxide membranes over cavities using ion-cut layer transfer, IEEE J. Microelectromech. Syst. 9 (4) (2000) 474–477.

[10] S. Pae, T. Su, J.P. Denton, G.W. Neudeck, Multiple layers of silicon-on-insulator islands fabrication by selective epitaxial growth, IEEE Electron. Device Lett. 20 (5) (1999) 194–196.

[11] B. Aspar, M. Bruel, H. Moriceau, C. Maleville, T. Poumeyrol, A.M. Papon, Basic mechanisms involved in the smart-cut process, Microelectron. Eng. 36 (1997) 233–240.

Biographies

Jiangang Du received BSEE degree in measurement and instrument from Xidian University,China in 1996, and MSME in manufacturing and automation from Xi’an Jiaotong University, China in 2000, respectively. Since 2000, he has been working in Dr. Darrin Young’s research group of MEMS as a research assistant. He is a PhD Case Prime Fellow at Case Western Reserve University. He is currently a student member to the Material Research Society (MRS) and Institute of Electrical and Electronics Engineers (IEEE). His current research interests are in the area of semiconductor-on-insulator (SOI) fabrication technology, silicon carbide (SiC) design and fabrication process, harsh environment sensing technology development, and wide-band semiconductor material applications.

Dr. Wen H. Ko received his BSEE from Xiamen University of China in 1946, and his MS and PhD in EE from Case Institute of Technology, Cleveland, OH, USA, in 1956 and 1959, respectively. He has been a faculty member of Electrical Engineering and Biomedical Engineering Departments at Case Western Reserve University (CWRU) Cleveland, OH, USA from 1959 to 1993. He became a Professor Emeritus in EE of CWRU in July 1993.

Dr. Ko has 21 patents and 317 publications, with 131 in referenced journals, in areas of solid state electronics, micro-sensors and actuators; bio-medical instrumentation, implant electronics and control system design.

Dr. Ko is a fellow of IEEE and American Institute of Medical and Biological Engineering. He is on the editorial board of Sensors and Actuator, Micro-system Technologies, Telemetry and Patient Monitoring (1974–1984), and Medical Progress through Technology (1983–1988). He was the chairman of International steering committee on solid state sensors and actuators conferences from 1983 to 1987 and the chairman of the international steering committee on chemical sensor meetings from 1991 to 1993. He received the Career Achievement Award in the Transducer 97 conference in Chicago, USA. He is the president of the Transducer Research Foundation that sponsored the Hilton Head Workshops on Sensors and Actuators in America, since 1992.

Darrin J. Young received his BS, MS, and PhD degrees from the Department of Electrical Engineering and Computer Sciences at University of California at Berkeley in 1991, 1993, and 1999, respectively. Dr. Young joined the Department of Electrical Engineering and Computer Science at Case Western Reserve University as an assistant professor in 1999. His research interests include MEMS design and fabrication, and integrated analog circuits design for wireless communications, sensing, biomedical implant, and general industrial applications.