2 GHz CMOS Voltage-Controlled Oscillator with Optimal Design of Phase Noise and Power Dissipation

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***Abstract*—An RF VCO design optimization strategy to achieve low phase noise and low bias current is presented for a cross-coupled *LC*-tuned CMOS oscillator topology. The impact of differential pair transistors' mode of operation and loading effects on the oscillator phase noise are investigated. The study shows that an optimal trade-off between thermal-noise-induced phase noise and DC power dissipation can be achieved when the oscillation amplitude is designed to set the differential pair transistors to operate at the boundary between saturation and triode regions. This design technique is employed to demonstrate a 2 GHz VCO achieving a low phase noise of -103 dBc/Hz at 100 kHz offset frequency while dissipating 2.67mA bias current from a 1.8V supply in a standard 0.18 µm CMOS process. The optimization strategy can be applied for other VCO design architectures to further enhance wireless communication system performance and battery lifetime.**

***Index Terms*—RF VCO, Low phase noise VCO, Low power VCO, VCO design optimization.**

I. Introduction

Radio-frequency (RF) voltage-controlled oscillators (VCOs) are key components in wireless communication systems with a constant demand for improved phase noise at minimal power consumption. Substantial research efforts have been devoted to achieve low oscillator phase noise by advancing component technologies such as quality factors (*Qs*) of inductors and varactors [1]-[3], improving oscillator topologies [4], resonator architectures [5], noise filtering techniques [6], device sizing [7], and post-processing [8]-[9]. Many studies on phase noise mechanisms are reported [4], [10]-[13]. Current-limited and voltage-limited regions of operation with optimal performance at the boundary between the two regions are identified [14]-[16]. While incorporating these technology advancements and design techniques into an oscillator's implementation, most low noise VCOs, however, rely on developing large oscillation signal amplitudes, thus causing an excessive current dissipation, which unfavorably shortens the battery lifetime of hand-held wireless communication devices.

In this paper, we report on the design and characterization of a 2 GHz CMOS low phase noise cross-coupled *LC*-tuned VCO with substantially reduced current dissipation compared to other published work exhibiting comparable phase noise and oscillation frequencies. This work highlights the importance of the differential pair transistors' mode of operation and the impact of transistors' loading effects on the quality factor of the *LC* tank. The experimental measurement results demonstrate that an optimal trade-off between the thermal-noise-induced phase noise and power dissipation can be achieved when the oscillation amplitude is designed to ensure the differential pair transistors operate at the boundary between saturation and triode.

II. VCO Performance Dependence on Transistors' Mode of Operation

Fig. 1 presents the prototype VCO architecture chosen as a research vehicle.

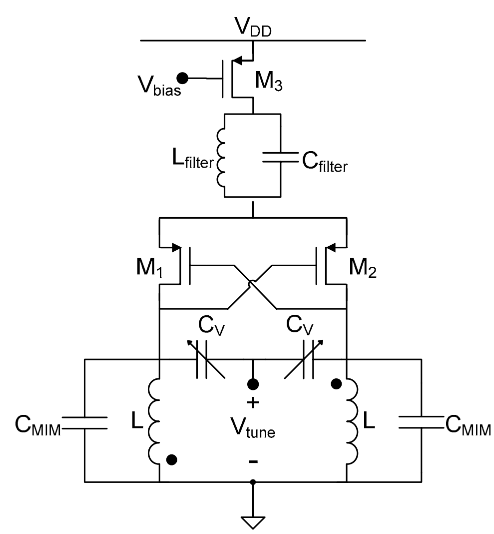

Fig. 1. RF VCO architecture.

The oscillator consists of cross-coupled differential pair transistors (M_1 and M_2) loaded with an *LC*-tuned tank.

The oscillator is designed to tune from 1.8 GHz to 2 GHz for typical cellular telephony applications. An extended tuning range can be obtained by adjusting the ratio between the varactor capacitance and fixed capacitance in the tank. PMOSFETs are employed in the design due to their low 1/*f* noise characteristics, critical for minimizing close-in phase noise. The oscillator *LC* tank is composed of a single three-turn center-tapped differential inductor [17] with an inner radius of 150 μm and trace width and spacing of 30 μm and 3 μm, respectively, and a capacitive network of MOS varactors and MIM capacitors. The inductor exhibits a differential inductance of 4.6 nH with a *Q* of 15 at 2 GHz. P-channel MOS capacitors are used as varactors for tuning the oscillator frequency. The varactors are biased in the depletion region to achieve a capacitance range from 2.4 pF to 1.6 pF at V_{GB} of -0.4V and -1.1V, respectively, while maintaining a high quality factor of over 30. To obtain the desired VCO frequency tuning range, additional high-*Q* MIM capacitors of 225 fF are included in the tank. Another parallel *LC* tank consisting of L_{filter} and C_{filter}, tuned to twice of the operating frequency ($2f_0$ = 3.8 GHz), is employed to suppress the up-conversion mechanism of the baseband noise from the biasing transistor (M_3), as proposed in [6], to minimize phase noise at low offset frequencies near the carrier.

Properly designing the differential pair transistors' mode of operation is crucial for achieving a low phase noise performance at minimal core bias current. Leeson's phase noise equation [18] suggests that low phase noise performance can be achieved by enhancing the RF power or oscillation signal amplitude through increasing the oscillator core bias current. However, designs aiming for a large oscillation swing with high current dissipation typically drive the differential pair transistors into a deep triode region, which severely degrades the oscillator loaded tank impedance and quality factor. High-*Q* tanks are especially prone to this type of operation. Fig. 2(a-c) presents an intuitive graphical illustration in describing the importance of ensuring the differential pair transistors to operate strictly in the saturation region. Fig. 2(a) shows the RF signal power versus bias current on a logarithmic scale. Note that in the saturation region the signal power increases as a function of square of the bias current, I^2. Once the bias current reaches to a level where the single-ended peak-to-peak oscillation amplitude exceeds the threshold voltage of the differential pair transistors, the active devices enter the triode region for a portion of the oscillation period. As the amplitude is further increased, the differential pair spends more of a period operating in triode, where the RF power does not increase as I^2 due to the degraded tank impedance as depicted in Fig. 2(a). The thermal noise contribution of the biasing transistor, M_3, typically dominates the VCO phase noise, which increases with its small-signal transconductance; hence, the square root of the bias current. Once the differential pair transistors enter the triode region, degraded tank impedance results in an output noise power profile with a reduced slope of less than $I^{1/2}$, as illustrated in Fig. 2(b). Combining Fig. 2(a) and Fig. 2(b) produces an oscillator phase noise profile as depicted in Fig. 2(c), indicating a dependence of $I^{-3/2}$ in the saturation region. A further increase of bias current results in a negligible phase noise improvement in the triode region. Therefore, an optimal oscillator design trade-off between an achievable low phase noise and bias current can be obtained by ensuring the differential pair transistors do not operate in the triode region. This thus calls for a single-ended peak-to-peak oscillation amplitude equal to the threshold voltage of the differential pair transistors for the chosen VCO topology.

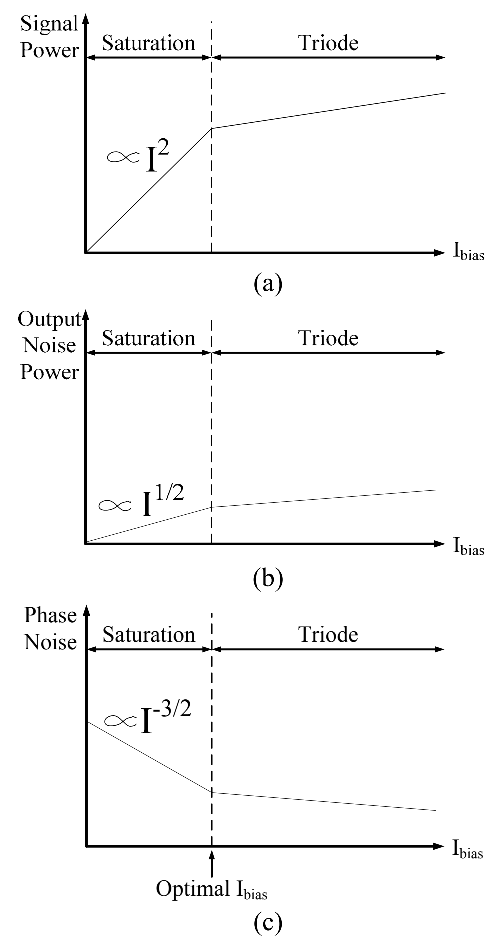

Fig. 2. Graphic analysis as a function of bias current.

III. Prototype RF VCO Design

A prototype RF VCO is designed in the TSMC 0.18 µm 1.8V non-epi process. Based on the components values described in Section II, the loaded *LC* tank impedance exhibits 230 Ω in the designed frequency range. Therefore, a DC bias current of 2.67mA is required for obtaining a single-ended peak-to-peak oscillation amplitude of 0.8V (the value of the PMOS threshold voltage with body effect). W/L of 64 µm / 0.18 µm for the differential pair transistors are thus needed to achieve a small-signal loop gain of 2 to ensure a proper oscillation startup. The biasing transistor is sized at 64 µm / 0.48 µm. The non-minimal channel length is selected to minimize the device 1/*f* noise contribution. The W/L is designed to be as small as allowed to ensure its operation in saturation while minimizing its thermal noise contribution to the oscillator phase noise. L_{filter} of 4.28 nH and C_{filter} of 410 fF are employed to achieve a resonance of 3.8 GHz for suppressing the up conversion mechanism of the base band noise from the biasing transistor.

IV. Measurement Results

Fig. 3 presents the micrograph of the VCO chip occupying an area of 1 mm x 1 mm including pads. The *LC* tank inductor occupies an area of approximately 550 µm x 550 µm.

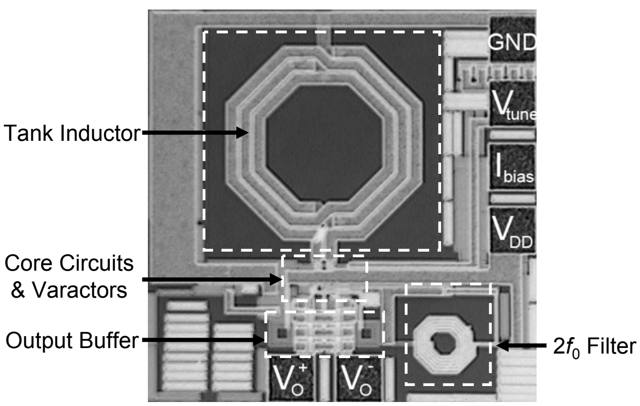

Fig. 3. Fabricated VCO micrograph.

The oscillator core is interfaced with an on-chip buffer, which exhibits an attenuation factor of 0.25 and is properly matched to 50 Ω impedance for external characterization. The VCO is tunable from 1.8 GHz to 2.0 GHz with 0.7V (0.4V < V_{tune} < 1.1V). Fig. 4 shows the oscillator output power spectrum at 2 GHz, displaying -10 dBm RF power with 2.67mA bias current dissipation from a 1.8V supply. The measured time domain waveform of the buffered oscillator output signal with a peak-to-peak amplitude of 216mV is shown in Fig. 5. This corresponds to an internal single-ended oscillation peak-to-peak amplitude of 0.8V, which matches the initial design objective.

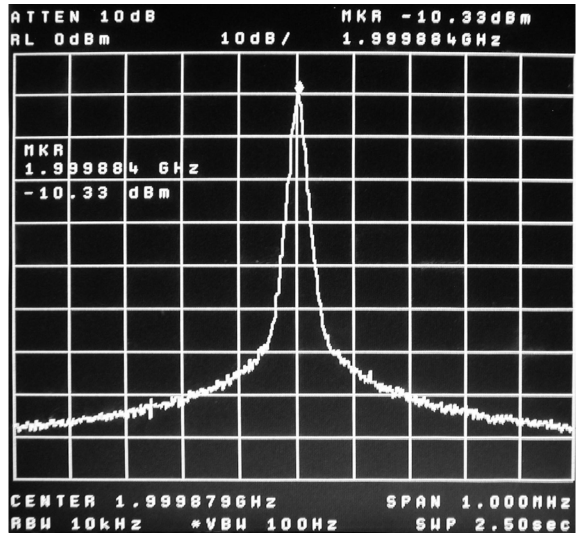

Fig. 4. Measured VCO output power spectrum at 2GHz.

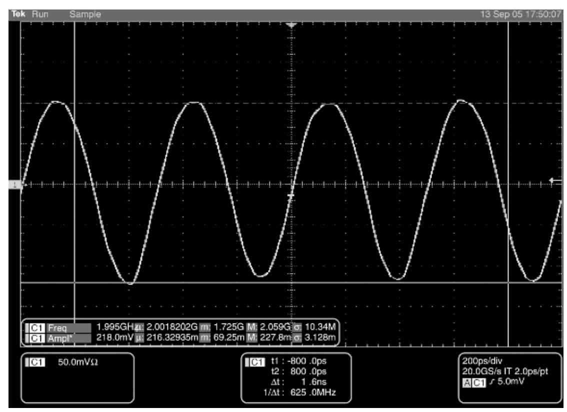

Fig. 5. Measured VCO output waveform at 2GHz.

The oscillator achieves a phase noise of -103 dBc/Hz at a 100 kHz offset from the 2.0 GHz carrier and reaches -125 dBc/Hz at 2 MHz offset frequency, limited by the noise floor of the measurement equipment. Fig. 6 plots the measured phase noise at 100 kHz offset frequency as a function of the oscillator bias current for center frequencies of 1.8 GHz, 1.9 GHz, and 2.0 GHz. The plot shows that a low phase noise is reached at the optimally designed bias current of 2.67mA. At this current level, the differential pair transistors are operated strictly in the saturation region when they are on. Further increase in bias current drives the transistors into triode without any significant phase noise improvement. The phase noise measured beyond 2.67mA of bias current exhibits a variation less than 1 dB. The measurement also shows a 4-5 dB phase noise difference between the bias currents of

1.67mA and 2.67mA, thus following the phase noise profile of $I^{-3/2}$, as predicted in Fig. 2(c), within the saturation region.

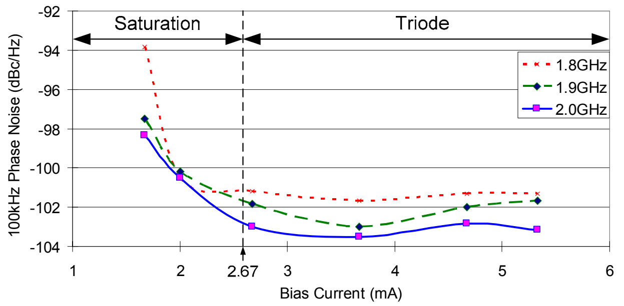

Fig. 6. Measured VCO phase noise at 100 kHz-offset frequency vs. bias current for center frequencies of 1.8GHz, 1.9GHz, and 2.0GHz.

The oscillator performance can also be characterized by using a figure of merit (FOM), which takes into account the phase noise, center frequency, offset frequency, and DC power dissipation [19]. The calculated VCO FOM with a center frequency of 2 GHz and offset frequency of 100 kHz versus bias current is shown in Fig. 7, indicating that the best FOM of -182.2 dBc/Hz/mW of the prototype oscillator is achieved at the optimal bias current of 2.67mA.

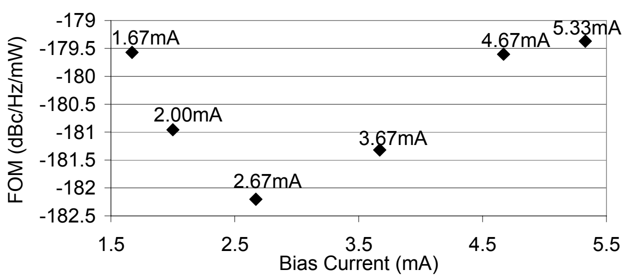

Fig. 7. Prototype VCO FOM vs. bias current.

V. Conclusion

An RF VCO design optimization strategy to achieve low phase noise and low bias current is presented for a cross-coupled *LC*-tuned CMOS oscillator topology. The study shows that an optimal trade-off between thermal-noise-induced phase noise and DC power dissipation can be achieved when the oscillation amplitude is designed to set the differential pair transistors to operate at the boundary between saturation and triode. A prototype VCO is implemented in a standard 0.18 μm CMOS process, achieving a phase noise of -103 dBc/Hz at a 100 kHz offset frequency from a 2 GHz carrier while dissipating 2.67mA from a 1.8V supply. The optimization strategy can be applied to other VCO design architectures for further performance enhancement.

Acknowledgement

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