

# A Micromachined RF Low Phase Noise Voltage-Controlled Oscillator For Wireless Communications

Darrin J. Young,<sup>1</sup> Bernhard E. Boser,<sup>1</sup> Vincent Malba,<sup>2</sup> Anthony F. Bernhardt<sup>2</sup>

<sup>1</sup>Department of Electrical Engineering and Computer Sciences,  
University of California, Berkeley, California 94720

<sup>2</sup>Lawrence Livermore National Laboratory, Livermore, California 94551

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**ABSTRACT:** An RF low phase noise voltage-controlled oscillator is implemented with micromachined IC-compatible variable capacitors and three-dimensional coil inductor. Unlike conventional on-chip passive devices, the micromachined variable capacitors achieve a high- $Q$  value above 60 at 1 GHz with a 15% tuning range for a nominal 2 pF capacitance with 3 V tuning voltage. Three-dimensional inductors minimize the substrate loss and achieve a  $Q$  of 30 at 1 GHz with a 4.8 nH inductance. Both passive components are fabricated on silicon substrates and thus amenable to monolithic integration with standard IC process. The prototype VCO exhibits  $-136$  dBc/Hz phase noise at 3 MHz offset frequency from the carrier, suitable for most wireless communication applications, in particular GSM. The VCO is tunable from 855 MHz to 863 MHz, limited by the test set-up. © 2001 John Wiley & Sons, Inc. *Int J RF and Microwave CAE* 11: 285–300, 2001.

**Keywords:** RF MEMS; micromachining; micromachined passive components; high- $Q$  RF devices; tunable capacitors; three-dimensional devices; coil inductors; RF VCOs; low phase noise VCOs

## I. INTRODUCTION

The increasing demand for wireless communication applications, such as cellular telephony, cordless phones, wireless data networks, two-way paging, global positioning systems, etc., motivates a growing interest in building miniature wireless transceivers with multistandard capabilities. Such transceivers will greatly enhance the convenience and accessibility of various wireless services. Increasing the level of integration to include passive devices is important for reducing the overall form-factor and ultimately supporting multiple standards in a single miniature

transceiver. Highly integrated transceivers, compared to conventional designs, will also result in reduced package complexity, power consumption, and cost.

At present, most wireless transceivers rely on a large number of discrete frequency-selection components, such as radio-frequency (RF) band-pass filters, intermediate-frequency (IF) channel-selection filters, RF voltage-controlled oscillators (VCOs), quartz crystal oscillators, solid-state switches, etc., to perform the necessary analog signal processing. These off-chip devices occupy a majority of the transceiver area, severely restricting miniaturization.

Micromachining offers a potential solution to integrate these discrete frequency selection components onto silicon substrates. Off-chip

Correspondence to: Darrin Young; e-mail: div@po.cwru.edu.

macroscopic devices can be replaced by on-chip microelectromechanical versions. Band-pass filters at RF and IF, low-frequency oscillators with high spectral purity intended for reference signal generators, and RF switches have been demonstrated with a size reduction of a few orders of magnitude [1–6]. Further research is still needed to enhance the performance of these devices.

Micromachining technology is also attractive for implementing on-chip high-quality RF variable capacitors and inductors, which are not available in conventional integrated circuit (IC) processes. Such devices can be used, for example, in low-noise amplifier and power amplifier matching networks and also for implementing monolithic low-noise VCOs. The quality factor of these passive components ultimately determines an oscillator phase noise performance, a critical parameter for a high-performance communication system.

This article focuses on the design and fabrication of silicon-based on-chip micromachined variable capacitors and inductors, and RF VCOs employing these passive components to achieve the stringent performance requirements for typical wireless applications. First, the requirements of RF VCOs for high-performance wireless systems are presented. The design and fabrication of high- $Q$  micromachined all-aluminum variable capacitors and three-dimensional coil inductors are described in Sections III and IV, respectively. Phase noise characteristics in a micromachined LC-tuned oscillator are examined in Section V. Section VI presents the design and measurement results of two prototype micromachined RF low phase noise VCOs.

## II. RF LOW PHASE NOISE VCO

A wireless transceiver mainly performs two functions, reception and transmission. In a reception mode, an RF VCO is used to convert the high-frequency incoming signal to a low-frequency band, where further signal processing techniques are applied to extract the desired information, for example human voice or data. In a transmission mode it performs the opposite function, converting the low-frequency information onto a high-frequency carrier and transmitting through the air medium. Most of wireless communication systems currently operate in the low Gigahertz range and require VCOs to achieve a tuning range of approximately 5% of the carrier frequency.

The specified stringent conditions on strong out-of-channel received signals demand an extremely low phase noise performance for the RF VCO in a receiver. For example, a requirement of  $-136$  dBc/Hz at 3 MHz offset frequency from the carrier must be achieved to satisfy the worst case interfering condition for GSM, a common cellular telephony application [7, 8].

Conventional VCO designs rely on an off-chip LC-tuned tank circuit with a quality factor close to 20 to achieve the low phase noise performance. Typical element values are on the order of 2 pF for the capacitor and 5 nH for the inductor. Frequency tuning is achieved through varying the depletion width of the capacitor, commonly called varactor diode. A capacitance change of at least 20% is needed to cover the tuning range. A hyperabrupt junction doping profile through a special epitaxial process is typically employed to achieve the tuning requirement with high  $Q$  factors around 50 at 1 GHz [9]. Specially made discrete coil inductors obtain high  $Q$ s of at least 30 at the same frequency [10]. Unfortunately, these approaches have proven difficult to realize in a monolithic silicon IC form. External components are thus needed for oscillator implementations, which result in a large size hindering the transceiver miniaturization.

RF VCO designs based upon integrated ring oscillator topologies [11] cannot achieve the stringent low phase noise requirement because this type of oscillator has an effective  $Q$  value about 1. The phase noise is primarily a function of power dissipation rather than electronic device characteristics [12]. Therefore, little improvement is expected from future technology scaling.

On-chip silicon PN-junction-based variable capacitors along with spiral inductors have been employed to implement monolithic VCOs [13–16]. However, the achieved phase noise performance falls well short of the cellular telephony requirements. This is due to the low quality factors, typically below 10 at 1 GHz for the capacitors and around 3 for the inductors, caused by an excessive series resistive loss and substrate loss at high frequencies [17]. Therefore, on-chip high- $Q$  passive components are highly critical for realizing monolithic high-performance RF VCOs. In the next two sections, new solutions based upon microelectromechanical technologies will be presented to realize on-chip high- $Q$  variable capacitors and inductors that achieve the stringent requirements for cellular telephony applications.

### III. SURFACE-MICROMACHINED VARIABLE CAPACITORS

#### A. Capacitor Description

Figure 1 presents the top and cross section views of a micromachined variable capacitor. It consists of 1  $\mu\text{m}$ -thick aluminum plate suspended in air nominally 1.5  $\mu\text{m}$  above the bottom aluminum layer and anchored with four mechanical folded-beam suspensions acting as springs. The folded suspensions have the advantage of being free to expand or contract if residual stress is present in the structure, thus relaxing the film stress and hence reducing warpage [18]. The symmetry avoids a systematic tilt of the device. Etch holes of 2  $\mu\text{m}$  by 2  $\mu\text{m}$  size spaced 10  $\mu\text{m}$  apart ensure a complete removal of the sacrificial material for releasing the microstructure. The chosen plate size of 200  $\mu\text{m}$  by 200  $\mu\text{m}$  and 1.5  $\mu\text{m}$  nominal air gap result in a nominal capacitance value of approximately 200 fF. Thus a large capacitance can be obtained through a parallel connection of multiple devices. These capacitor dimensions represent a compromise between the achievable capacitance value and the maximum structure size

that can be fabricated reliably without an excessive warping. The warping is mainly caused by the thermal expansion mismatch between the sacrificial material, which is photoresist in the current process, and the top aluminum layer. The elevated temperature during the deposition and subsequent cooling to the room temperature further contribute to a built-in strain gradient in the aluminum film and cause the structure to warp after removal of the sacrificial layer. Difficulties in removing the sacrificial material preclude a reduced air gap despite the potential for an increased capacitance density and reduced tuning voltage. A DC bias voltage applied across the capacitor results in an electrostatic pull-down force and consequent reduction of the air gap. The suspended plate can be pulled down at most by one-third of the original gap size before the pull-down force exceeds the mechanical restoring force, causing the plate to be pulled all the way to the substrate. This deflection range corresponds to a maximum 50% increase in the capacitance value. However, parasitic capacitances associated with the device and interconnect will result in a reduced tuning range.

Despite the better mechanical properties and extensive experience with polysilicon microstructure fabrication [19], aluminum is chosen as the structural material in the variable capacitor design for the following reasons. First, its low sheet resistance is critical to minimize the ohmic losses and guarantee an adequate quality factor even at high frequencies. The second key advantage of aluminum is the low processing temperature of only 150°C for the proposed fabrication procedure, as will be demonstrated in this section. Because of the low thermal budget, the variable capacitors can be fabricated on top of wafers with completed electronic circuits without degrading the performance of active devices. This is particularly crucial in applications such as RF where the availability of the most recent IC technology is a key competitive advantage. The inferior mechanical properties of aluminum compared to polysilicon are not critical for VCO applications because the suspended microstructure does not require a large displacement.

In RF transceivers, the DC tuning voltage is typically limited to 3.3 V or less by the supply voltage. Thus with a 1.5  $\mu\text{m}$  nominal air gap and a 200  $\mu\text{m}$  by 200  $\mu\text{m}$  plate size, a mechanical suspension with a spring constant,  $k_m$ , of 3.8 N/m is required for a 3.3 V operation. This corresponds

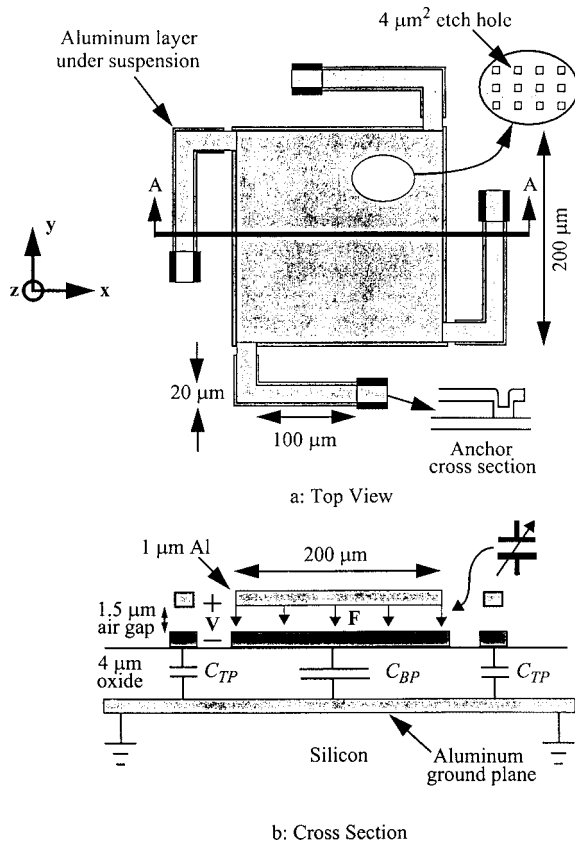


Figure 1. Micromachined variable capacitor.

to a mechanical resonant frequency of approximately 30 KHz. The suspension employed in the current design consists of four folded beams of 100  $\mu\text{m}$  length and 20  $\mu\text{m}$  width as shown in Figure 1a. By designing the suspension with an increased compliance, a further reduced tuning voltage requirement can be accommodated. This presents an important advantage over the conventional varactor diodes with their tuning ranges being a strong function of the supply voltage. The mechanical variable capacitor is, therefore, attractive for low-power RF applications with the continuing supply voltage reduction. Typical radio frequencies of interest are almost six orders of magnitude large than the mechanical resonant frequency, thus the suspended plate of the variable capacitor is virtually insensitive to RF signals. This characteristic results in extremely linear behavior compared to the conventional varactor diodes, critical for low-distortion filtering applications. Since the RF signal amplitude is not limited by forward-biasing, the device can sustain a large signal swing, attractive for implementing a low phase noise VCO and also for tuning wireless transmitters with high output power requirements. The signal amplitude is ultimately limited by the RF voltage-induced pull-down effect.

The parasitic capacitances,  $C_{\text{TP}}$  and  $C_{\text{BP}}$ , between the top and bottom plates of the variable capacitor and the substrate are shown in Figure 1b. In a typical VCO design, the bottom plate of the capacitor is grounded and  $C_{\text{BP}}$  is therefore shorted. However, the top-plate parasitic,  $C_{\text{TP}}$ , appears in parallel with the variable capacitor. This not only reduces the tuning range, but can also lower the quality factor of the overall capacitor because  $C_{\text{TP}}$  suffers from the substrate resistive loss causing a low  $Q$  value. These problems are alleviated with a separated aluminum layer directly on the silicon substrate isolated from the capacitor bottom plate with a 4  $\mu\text{m}$  thick oxide. The thick oxide minimizes the value of the parasitic capacitances. The aluminum layer shields the parasitics from the lossy substrate, thus ensuring a high- $Q$  factor. In this design the bottom plate aluminum extends from the anchors under the suspensions up to the edge of the movable plate, as shown in Figure 1a. This conservative design has been chosen to prevent the capacitors from shorting out when the suspensions touch the bottom plate. However, this causes a relatively large parasitic capacitance of approximately 220 fF for the four suspensions and thus reduces the tuning range. The capacitor

shorting has not been found in fabricated devices. Therefore, a modified layout which minimizes this parasitic capacitance will be used for future designs.

## B. Mechanical Thermal Noise

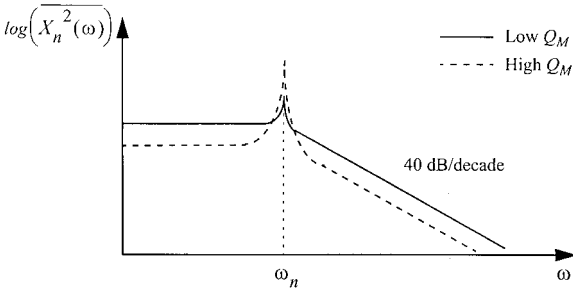
The suspended plate of a micromachined variable capacitor exhibits minute random vibrations due to collisions with molecules from the surrounding gas. These collisions generate a noise force commonly known as the Brownian noise in mechanical systems [20]. The thermal agitation of the suspended plate causes a capacitance variation, thus resulting in an additional output frequency jitter, or phase noise, when the capacitors are used for VCO tuning. The plate displacement noise power spectral density,  $\overline{X_n^2(\omega)}$ , can be determined and shown as

$$\overline{X_n^2(\omega)} = \frac{4kTb}{k_m^2 \left[ \left(1 - \frac{\omega^2}{\omega_n^2}\right)^2 + \frac{1}{Q_M^2} \frac{\omega^2}{\omega_n^2} \right]}, \quad (1)$$

where  $k$  is the Boltzman's constant,  $T$  is the absolute temperature,  $b$  is the damping coefficient due to the surrounding gas ambient and the internal dissipation of the system,  $\omega_n$  is the mechanical resonant frequency of the structure, and  $Q_M$  is the mechanical quality factor. For frequencies below and above  $\omega_n$ , Equation (1) evaluates approximately as  $4kT/mQ_M\omega_n^3$  and  $4kT\omega_n/mQ_M\omega^4$ , respectively, where  $m$  presents the mass of the suspended plate. At the resonance it is  $4kTQ_M/m\omega_n^3$ . Since in a typical micromachined variable capacitor design, the movable structure mass and mechanical spring constant are constrained by the fabrication technology and tuning voltage requirement,  $Q_M$  is therefore the only parameter through which the spectral density can be altered significantly. Increasing  $Q_M$  through decreasing the damping coefficient concentrates the thermal noise at  $\omega_n$  while reducing it elsewhere as shown in Figure 2. The impact of this noise on the phase noise performance of a micromachined VCO will be illustrated in Section V.

## C. Fabrication Process

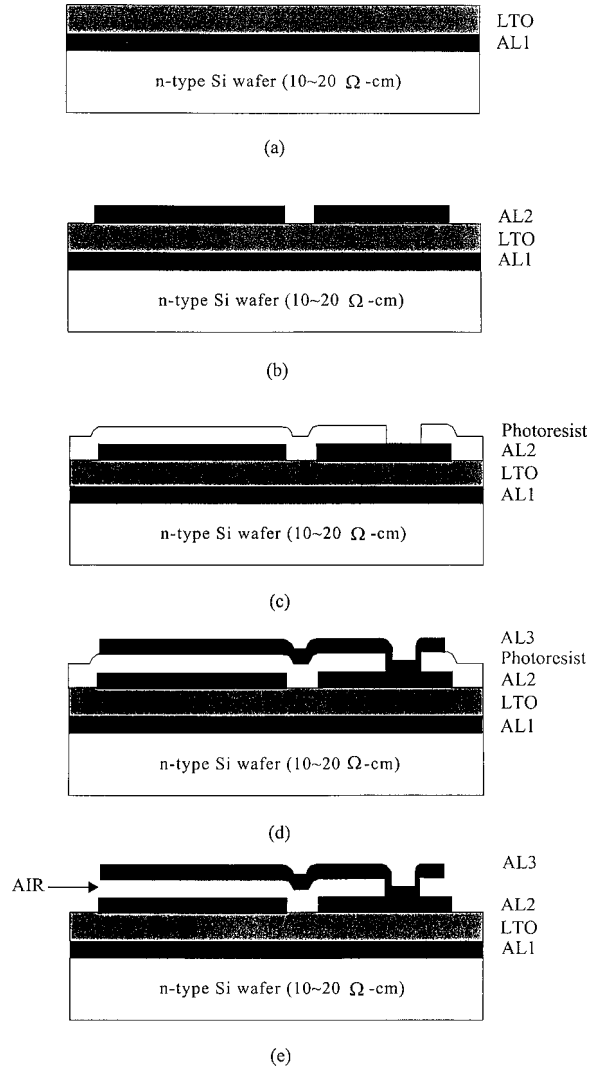
The experimental devices have been fabricated on a bare silicon wafer. Figure 3 illustrates the process flow. First, a 1- $\mu\text{m}$  thick aluminum film is sputtered onto the bare silicon wafer to form a low resistance ground plane. Next, a 4  $\mu\text{m}$



**Figure 2.** Effect of  $Q_M$  on displacement noise spectral density.

low-temperature oxide is deposited (Figure 3a). The bottom plate of the capacitor and interconnect trace consist of another  $1\text{-}\mu\text{m}$  thick sputtered aluminum film (Figure 3b). A wet etching step is chosen to pattern this layer since the lateral dimensions of the structure are not critical. Next a  $1.5\text{-}\mu\text{m}$  thick photoresist is deposited as a sacrificial layer. This material offers an excellent control of thickness and uniformity. Furthermore, it is photo-definable and easy to process. Contact windows to the bottom aluminum are opened in the resist (Figure 3c). It is then baked at  $120^\circ\text{C}$  for 45 minutes to prevent an out-gassing during the subsequent deposition of the top aluminum layer. An increased baking time will result in a hardening of the resist and consequent difficulties in its removal. The final  $1\text{ }\mu\text{m}$  aluminum layer is sputtered at a reduced power level and also wet etched since a plasma dry etch will cause outgassing to the sacrificial layer. This layer forms anchors to the bottom aluminum inside the contact windows through the resist. (Figure 3d). In addition, it is also deposited on all interconnect traces to lower the resistance, not shown in this figure. At this point, the wafers are coated with a  $1\text{-}\mu\text{m}$  thick photoresist to protect against particulates during dicing. After dicing and removal of particulates, the protective resist is first etched away using a direct reactive ion etch. The sacrificial layer is then removed with an oxygen-based dry etch in a barrel reactor which offers an increased lateral etch rate, thus releasing the capacitor top plate (Figure 3e).

The oxygen gas pressure and plasma power must be set properly to ensure a complete removal of the resist and prevent the aluminum film from warping significantly. The structure heats up to approximately  $150^\circ\text{C}$  during the 180-minute long etch. An optimal pressure of 500 mTorr and 150 W power have been determined experimentally. The dry etching process virtually eliminates



**Figure 3.** Capacitor fabrication process flow.

the problem of the structure sticking to the substrate. This is an important advantage over the wet release procedure typically used with the polysilicon microstructures. Because of the low processing thermal budget, the variable capacitors can be fabricated on top of wafers with completed electronic circuits without degrading the performance of active devices.

#### D. Measurement Results

Figure 4 shows SEM micrographs of a single tunable capacitor. An optical inspection reveals doming of the capacitor top plate. The plate center and four corners are approximately  $0.5\text{ }\mu\text{m}$  above and below the nominal gap of  $1.5\text{ }\mu\text{m}$ . The warpage limits the maximum device size. Large capacitance value can be obtained by connecting

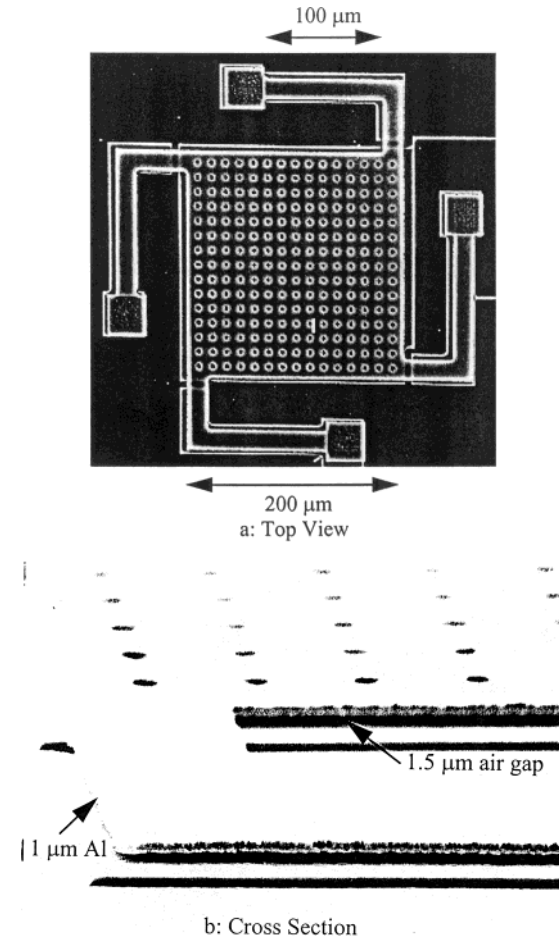


Figure 4. SEMs of fabricated micromachined capacitors.

several capacitors in parallel as shown in Figure 5. With a 3 V tuning voltage, the capacitance value can be varied between 2.04 pF to 2.35 pF. This corresponds to a tuning range of 15% shown in Figure 6. The tuning range is limited by the device parasitic capacitances described previously and can be extended through an appropriate layout modification. Aside from the capacitance, the quality factor is the most important electrical parameter of the structure. Figure 7 shows the

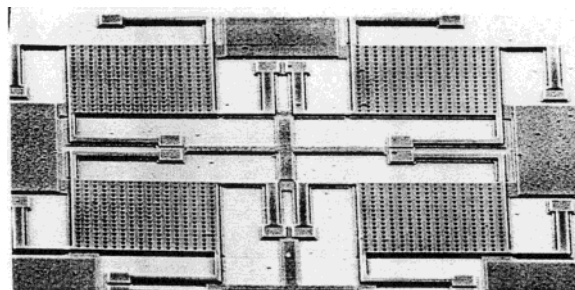


Figure 5. Four parallel microstructures.

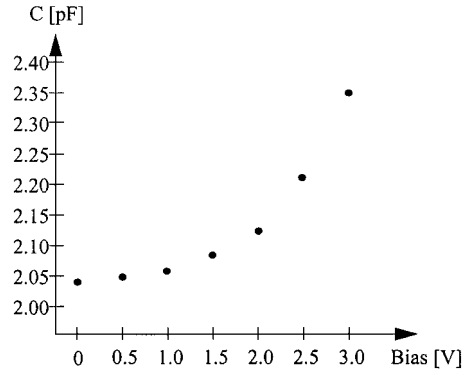


Figure 6. C-V measurement.

measured S11 curve in a Smith Chart for the four parallel capacitors. The S11 curve follows closely the lower half of the unit circle as is expected for a capacitor. At 1 GHz the series resistance is 1.2  $\Omega$  corresponding to a  $Q$  value of 62, limited by the resistive loss associated with the interconnect traces. This quality factor matches or exceeds that of discrete varactor diodes and is at least an order of magnitude larger than that of a typical junction capacitor implemented in a standard IC process.

#### IV. THREE-DIMENSIONAL ON-CHIP COIL INDUCTORS

##### A. Inductor Description

Figure 8 presents an SEM micrograph of a fabricated three-dimensional coil inductor on a silicon substrate. The fabrication process will be outlined below. The device consists of four-turn 5- $\mu\text{m}$  thick and 50- $\mu\text{m}$  wide copper traces electroplated around an insulating core. The core has a cross section area of approximately 650  $\mu\text{m}$  by 500  $\mu\text{m}$ . Compared to conventional on-chip spiral

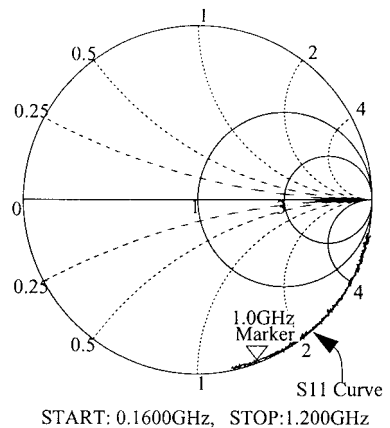
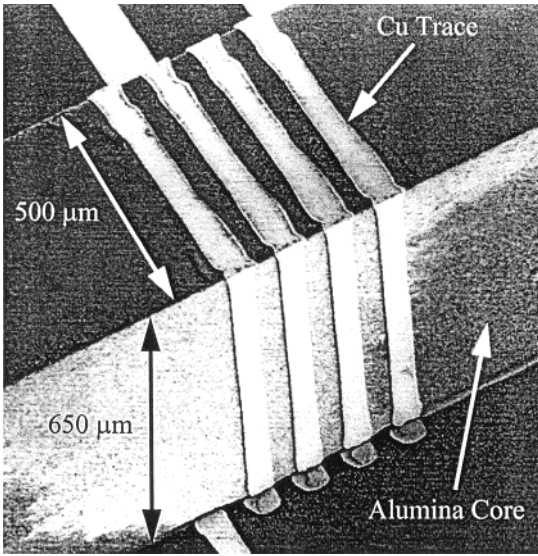


Figure 7. Measured S11 in a Smith Chart.



**Figure 8.** SEM of a fabricated three-dimensional coil inductor.

inductors, this geometry minimizes the coil area which is in close proximity to the substrate and hence the capacitive coupling. It thus results in a reduced substrate current loss at high frequencies and also an increased self-resonant frequency. Copper is selected as the trace metal for its low sheet resistance, critical for achieving a high- $Q$  factor, and its deposition simplicity through an electroplating process. The  $5\text{ }\mu\text{m}$  trace thickness is selected in this design because of the copper skin depth around  $2.4\text{ }\mu\text{m}$  at 1 GHz. An increased metal thickness will further minimize the resistance. However, thicker metal traces are not used due to current processing constraints. The  $50\text{ }\mu\text{m}$  metal width represents a compromise between the trace resistance and capacitance to the substrate. A  $50\text{ }\mu\text{m}$  line spacing is used to avoid processing difficulties in this conservative design. Alumina is chosen as the core material because of its negligible loss tangent at high frequencies with a typical value around  $30 \times 10^{-4}$  at 1 GHz [21], another key parameter to ensure a high  $Q$ . The core width of  $500\text{ }\mu\text{m}$  is found experimentally to be the minimum that avoids tilting during its attachment to the bottom copper traces. Its height of  $650\text{ }\mu\text{m}$  is limited by the thickness of a commercially available alumina sheet from which the core is formed as will be described in this section. A higher three-dimensional structure will achieve a larger inductance value without significantly increasing the capacitance coupling to substrate, thus leading to an improved quality factor. However, the ultimate device height will be limited by packaging constraints.

With the device dimensions described above, three types of inductors with one, two and four turns are fabricated. Because the device cross-section is large compared to the length, the classical formula for solenoidal inductance calculation does not apply. The simulation with Maxwell 3D Field Simulator [22] predicts 4 nH, 7.5 nH, and 13.5 nH for the three designs. The measured inductances are 4.8 nH, 8.2 nH and 13.8 nH. These inductance values are adequate for RF applications at Gigahertz frequencies. Due to the limitation of the simulator, the three-dimensional inductors are simulated without including any substrate effects. Thus, the device resistances simulation only represents the metal trace resistances, which are approximately  $0.4\text{ }\Omega$ ,  $0.86\text{ }\Omega$ , and  $1.8\text{ }\Omega$  for the one-, two- and four-turn designs at 1 GHz, respectively, corresponding to ideal  $Q$  factors of 63, 55, and 47. The measured inductor  $Q$  factors, however, are less than the ideal values due to additional contact resistances and substrate loss.

## B. Fabrication Process

The experimental devices have been fabricated on a bare silicon wafer. Figure 9 illustrates the process flow. First, the wafer is passivated with a  $5\text{-}\mu\text{m}$  thick low-temperature oxide (Figure 9a). This layer isolates the three-dimensional inductor to be fabricated on top away from the silicon substrate. An increased oxide thickness will further minimize the capacitive coupling. However, a  $5\text{ }\mu\text{m}$  thickness is chosen because it represents a typical thickness available in a standard IC process. Then the bottom traces of the inductor are fabricated. For this purpose, a  $500\text{ }\text{\AA}$  titanium and  $3000\text{ }\text{\AA}$  copper seed layer are sputtered and covered by a  $8\text{-}\mu\text{m}$  thick electroplated photoresist. This photoresist layer, however, can also be deposited through a spin-on technique. The  $8\text{ }\mu\text{m}$  thickness is chosen due to the current photolithography constraint, thus limiting the thickness of the electroplated copper. The pattern of the bottom metal traces are transferred photolithographically. Contacts are opened after developing the photoresist (Figure 9b). This step is followed by a selective electroplating of  $5\text{ }\mu\text{m}$  copper traces. To prevent oxidation, the copper is passivated with two  $1000\text{ }\text{\AA}$  layers of electrolytic nickel and gold (Figure 9c). Finally the photoresist and copper/titanium seed layer are removed with a wet etch step, leaving the bottom metal traces of the inductor on the substrate (Figure 9d).

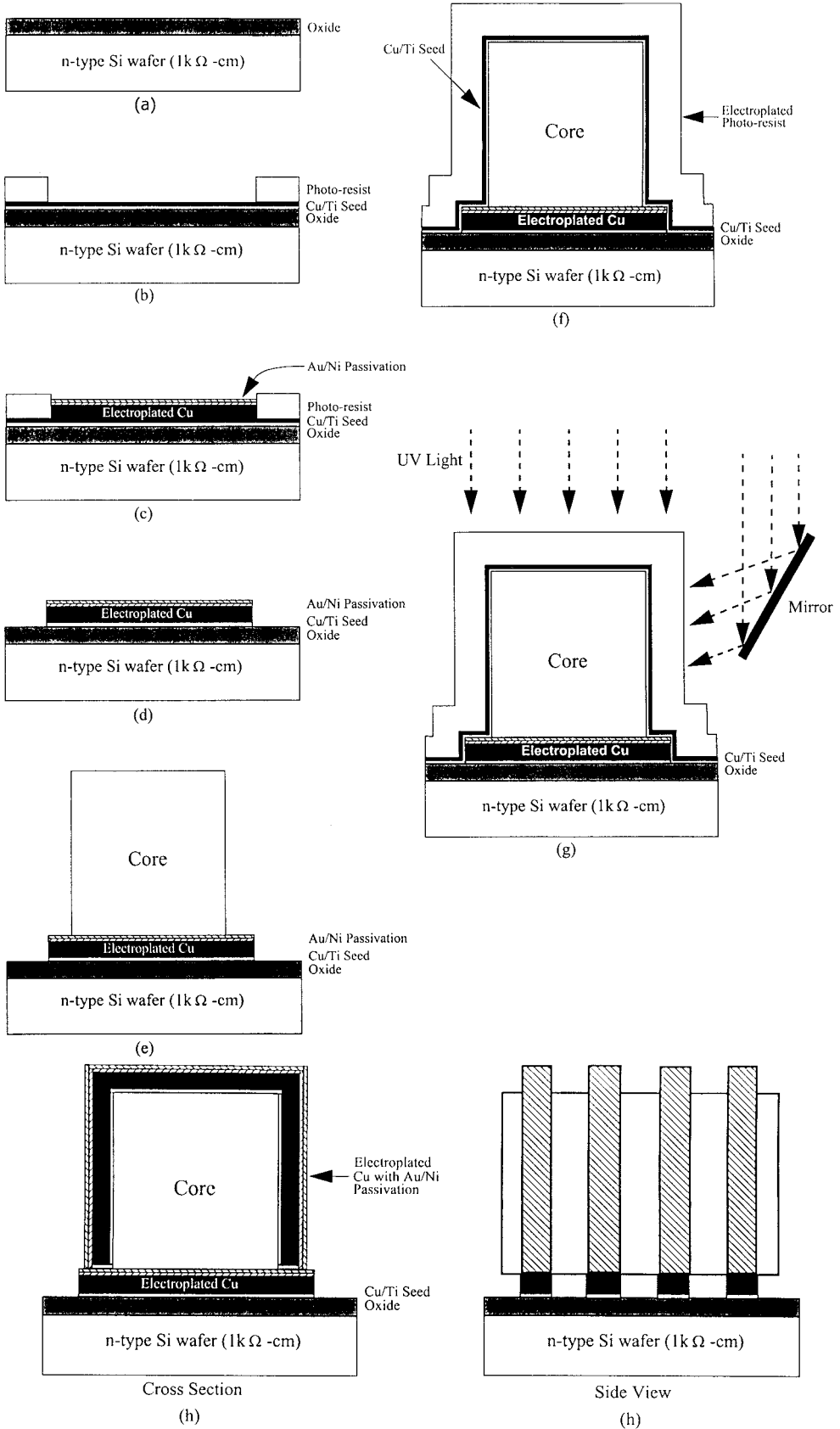


Figure 9. Inductor fabrication process flow.

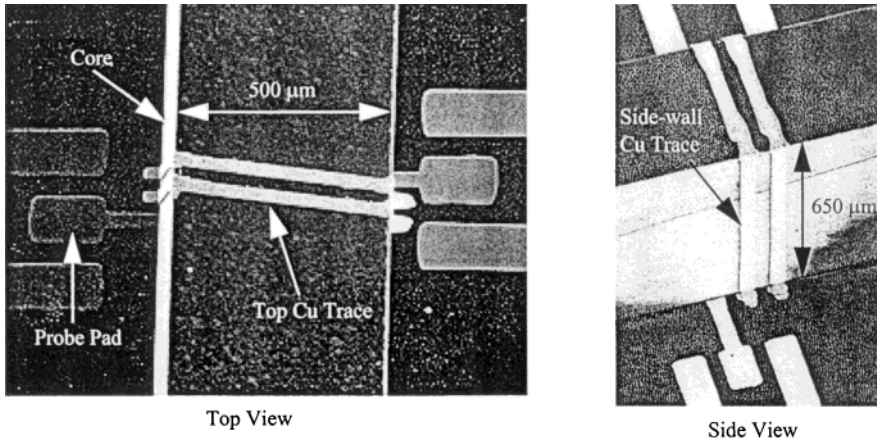


Figure 10. SEMs of a two-turn three-dimensional coil inductor.

The core of the inductor is formed from an alumina sheet, which is diced into 500- $\mu\text{m}$  wide strips. A 2% width accuracy is achieved by using a thin diamond grit blade on a commercial dicing saw. The strips are then manually centered on the bottom copper traces and baked at 170°C for 30 seconds, resulting in an adhesion to the substrate through adhesive materials placed at both ends of the core (Figure 9e). This manual placement technique is employed for fabricating the prototype devices. A batch fabrication method by using thick polyimide films will be considered for realizing the inductor cores in the future.

To fabricate the copper traces on the side and the top of the alumina core, the same process as for the bottom traces is used (Figure 9f). The photoresist electroplating step here is critical because it can conformally cover a complex surface such as the inductor core. The resist is exposed with a three-dimensional maskless direct-write laser lithography tool as illustrated in Figure 9g [23]. The laser beam can directly expose the resist on top of the core and is reflected by a mirror system to expose the sidewall. After developing the laser-exposed resist, 5- $\mu\text{m}$  thick copper traces are then electroplated along the sidewall and on top of the core. Electrolytic nickel and gold are deposited afterwards to prevent copper oxidation, followed by etching away photoresist and copper/titanium seed layer to complete the fabrication process. The final inductor is illustrated in Figure 9h. Because of the low processing temperature, the inductor can be fabricated on top of wafers with completed electronics without sacrificing the active device performance.

### C. Measurement Results

Figure 10 shows SEM micrographs of a fabricated two-turn three-dimensional inductor. The coil area above the silicon substrate is approximately 250  $\mu\text{m}$  by 500  $\mu\text{m}$ , comparable to that of a typical spiral inductor achieving a similar value. The two sets of ground-signal-ground probe pads are employed for measuring the device two-port S-parameters. Figure 11 shows the measured quality factor and inductance value as a function of frequency after de-embedding the parasitics from the probe pads. The device achieves an 8.2 nH inductance value with a  $Q$  factor of 16 at 1 GHz. This quality factor is substantially higher than that of a typical spiral inductor. Table I summarizes the performance of the fabricated devices. A  $Q$  of 30 at 1 GHz is achieved for the one-turn device. These performances represent a substantial improvement compared to the conventional spiral inductors. A patterned ground shield inserted between coil inductors and silicon substrate can potentially further improve the quality factor [24]. The devices are, therefore, suitable

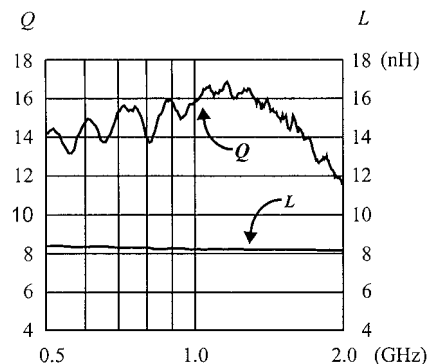


Figure 11. Measured  $Q$  and  $L$  for two-turn inductor.

**TABLE I. Performance Summary Table for Fabricated Three-dimensional Coil Inductors**

	One-turn	Two-turn	Four-turn
Inductance	4.8 nH	8.2 nH	13.8 nH
$Q$ at 1 GHz	30	16	16
$f_{\text{res}}$	>10 GHz	>10 GHz	>5 GHz
Silicon area	150 $\mu\text{m} \times 500 \mu\text{m}$	250 $\mu\text{m} \times 500 \mu\text{m}$	450 $\mu\text{m} \times 500 \mu\text{m}$

for building high-performance wireless communication circuits such as the RF low phase noise VCOs.

## V. VCO PHASE NOISE

In a conventional LC-tuned oscillator, the electrical thermal noise,  $1/f$  noise, and noise from the supply voltage and substrate contribute to the final phase noise [25]. A micromachine-based LC-tuned oscillator introduces an additional phase noise due to the mechanical-thermal vibration, also known as the Brownian motion, from the variable capacitors. The vibration of the suspended plates causes a variation in the capacitance value, hence, jitters (or phase noise) in the output frequency. This additional phase noise can be determined and expressed as

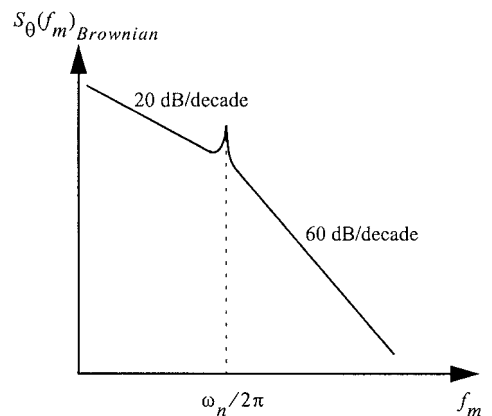
$$S_{\theta}(f_m)_{\text{Brownian}} = \frac{\overline{X_n^2(f_m)}}{8\left(\frac{1+\alpha}{\alpha}\right)^2 N x_o^2} \left(\frac{f_o}{f_m}\right)^2, \quad (2)$$

where  $\overline{X_n^2(f_m)}$  is the displacement noise power spectral density of the suspended plate described by eq. (1),  $x_o$  is the nominal air gap of the variable capacitor,  $N$  is the number of the parallel-connected micromachined capacitors,  $\alpha$  is the ratio between the nominal tank tunable capacitance and its parasitics,  $f_o$ , and  $f_m$ , are the oscillation frequency and offset frequency of interest, respectively. The effect of this noise is illustrated below with typical performance values.

The displacement noise power spectral density of the micromachined capacitor is constant below the mechanical resonant frequency,  $\omega_n$ , and decays at 40 dB per decade above  $\omega_n$  as shown in Figure 2. Therefore, the resulting phase noise profile decreases at 20 dB and 60 dB per decade below and above the offset frequency of  $\omega_n/2\pi$ , respectively, as illustrated in Figure 12 on a logarithmic scale. At  $\omega_n/2\pi$  offset frequency the phase noise is enhanced due to the peaking

in the capacitor displacement noise power spectral density at the mechanical resonance. Based upon eqs. (1) and (2), the Brownian motion induced phase noise can be determined at various offset frequencies. For a typical design condition of  $x_o = 1.5 \mu\text{m}$ ,  $m = 100 \text{ ng}$ ,  $Q_M \cong 1$  at 1 atm,  $\omega_n = (2\pi)(30 \text{ KHz})$ ,  $N = 4$ ,  $\alpha \cong 0.5$ , and  $f_o = 1 \text{ GHz}$ , the phase noise values at offset frequencies of 10 KHz, 100 KHz, and 3 MHz are calculated as  $-64 \text{ dBc/Hz}$ ,  $-105 \text{ dBc/Hz}$  and  $-194 \text{ dBc/Hz}$ , respectively. Typical wireless communication applications specify a low phase noise requirement at a relatively large offset frequency, for example  $-136 \text{ dBc/Hz}$  at 3 MHz offset for GSM. Therefore, the Brownian motion effect does not prevent the oscillators from achieving the required performance. However, if a close-in low phase noise is demanded for certain stringent applications, then this additional noise must be reduced. The Brownian motion induced phase noise can be suppressed by various methods as proposed below. Each approach has its limitations and trade-offs.

Using a micromachined capacitor with an increased plate size will reduce the displacement noise power spectral density thus suppressing the phase noise, provided that the mechanical resonant frequency remains constant for maintaining



**Figure 12.** Brownian motion induced phase noise profile.

the same tuning voltage. However, the warpage limits the maximum device size that can be fabricated reliably.

Connecting  $N$  micromachined capacitors in parallel will result in an overall displacement noise power spectral density of  $\overline{X_n^2(f_m)}/N$  due to an averaging effect, where  $\overline{X_n^2(f_m)}$  represents the corresponding spectral density for each individual capacitor. Therefore, an increased number of parallel-connected capacitors will reduce the phase noise. However, the value of  $N$  is ultimately limited by the total required capacitance in an oscillator. Using small capacitors with a reduced plate area will call for an increased number of parallel-connected capacitors to achieve the desired total capacitance. The final resulting phase noise, however, will remain approximately the same because the displacement noise power spectral density of each capacitor will increase due to the reduction of the suspended plate mass, provided that the mechanical resonant frequency is held constant to maintain the same tuning voltage.

Increasing the capacitor nominal air gap,  $x_o$ , will suppress the Brownian motion effect. The associated drawback is that an increased tuning voltage is needed. Reducing the ratio between the tunable capacitance and tank parasitics will improve the phase noise performance but at the expense of a narrowed tuning range.

Altering the capacitor displacement noise spectral density,  $\overline{X_n^2(f_m)}$ , can minimize the phase noise in certain regions. As shown in Figure 2,  $\overline{X_n^2(f_m)}$  can be shaped significantly through varying the structure mechanical quality factor,  $Q_M$ . Increasing  $Q_M$  by decreasing the ambient pressure reduces the spectral density away from the mechanical resonant frequency, thus resulting in a phase noise suppression as illustrated in Figure 13 on a logarithmic scale. However, at the mechanical resonance the noise is enhanced due to the increased  $Q_M$ . Therefore, depending upon applications, this phase noise shaping can potentially be attractive especially when there is no adjacent channel at  $\omega_n$  away from the desired channel. Besides all the suppression methods proposed above, a close-in low phase noise is achieved when the VCO is enclosed in a wide-band phase-locked loop (PLL). By extending the PLL loop bandwidth, an improved suppression on the close-in phase noise can be accomplished [26]. The PLL loop also suppresses the VCO frequency variation caused by low-frequency mechanical vibrations, thus minimizing capacitors microphonics effect.

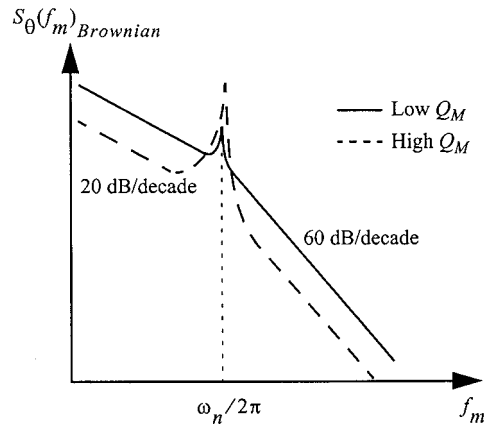


Figure 13. Effect of  $Q_M$  on Brownian motion induced phase noise.

## VI. PROTOTYPE MICROMACHINED RF VCO

This section presents the design and measurement results of two prototype micromachined RF voltage-controlled oscillators. In the first prototype, the micromachined variable capacitors and active electronics are realized on separate silicon substrates. They are attached to a test board and wire-bonded together with a commercially available discrete inductor to form the VCO. In the second version, a fabricated three-dimensional coil inductor is used to replace the discrete inductor. This hybrid approach is chosen to reduce the complexity of building the prototype VCOs. Because the three key components, the variable capacitor, inductor, and active electronics, are all fabricated on silicon wafers, they are in principle amenable to integration on the same substrate.

The prototype VCO configuration is shown in Figure 14. The Colpitt's oscillator topology is chosen as a testing vehicle because of its simplicity. The oscillator core electronics consist of  $M_1$  functioning as a common-gate amplifier with a small-signal transconductance of 30 mA/V, and capacitors  $C_1$  and  $C_2$  with 1 pF and 4 pF, respectively, to form a feedback path. Both capacitors are implemented by using metal-oxide-metal sandwiched layers to ensure a high  $Q$  factor. The discrete inductor has an 8.2 nH inductance value with a specified  $Q$  factor of 30 at 1 GHz. This inductance value is chosen to resonate with an overall capacitance estimated around 4.8 pF at 800 MHz. To minimize the tank loading, the oscillator output is taken between  $C_1$  and  $C_2$  and buffered through  $M_4$  for an external measurement. A 50  $\Omega$  resistor load is used at the output of  $M_4$  to achieve an impedance matching.

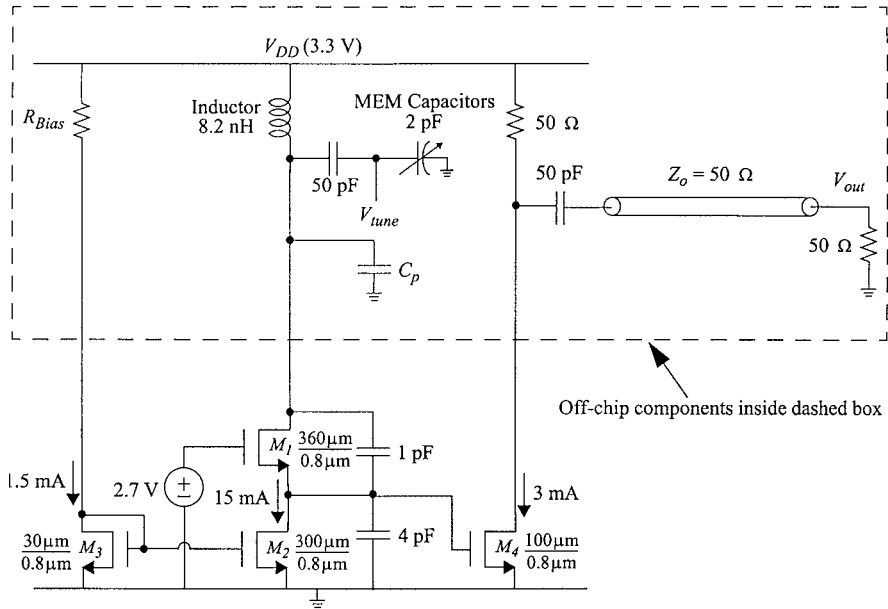


Figure 14. Prototype VCO configuration.

The VCO electronics are fabricated using HPs 0.8  $\mu\text{m}$  CMOS process. The die photo is shown in Figure 15, where  $M_1$  is placed adjacent to a bond pad through which the active electronics are interfaced to the LC tank. Every high-frequency signal pad is shielded by a metal layer underneath, which is then grounded through two adjacent bond pads on each side. This approach minimizes the substrate noise coupling and high-frequency signal feed through to the nearby bondwires used for DC bias. The shielding also ensures a high- $Q$  parasitic capacitance for the bond pad connected to the resonator, critical to achieve a low phase noise. A photograph of the prototype VCO test board is presented in Figure 16. A set of four parallel-connected micromachined variable capacitors on a silicon substrate is wire-bonded to the test board with the CMOS VCO electronics die and a discrete inductor to form the oscillator. The VCO oscillates at a center frequency of

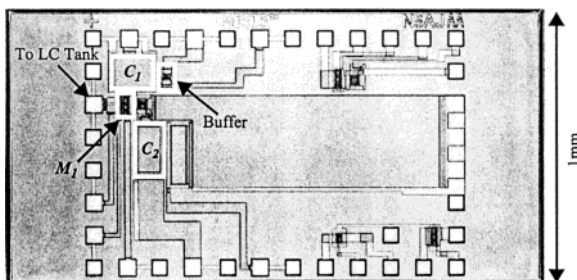


Figure 15. CMOS VCO electronics die photo.

714 MHz and can be tuned from 707 MHz to 721 MHz with 3 V. The center frequency is lower than the designed value of 800 MHz due to an excessive board parasitic capacitance, which also limits the VCO tuning range. Figure 17 shows the oscillator output power spectrum measured at 721 MHz with an estimated RF power of  $-2$  dBm developed in the LC tank. At 100 KHz offset frequency, a phase noise of  $-110$  dBc/Hz is achieved. To measure the VCO phase noise at 3 MHz offset frequency, a low noise-floor phase noise measurement system, HP 3048AR, is used. Figure 18 presents the measured phase noise plot of the prototype VCO, indicating that a phase noise of  $-139$  dBc/Hz is achieved at 3 MHz offset frequency. The low phase noise is due to the

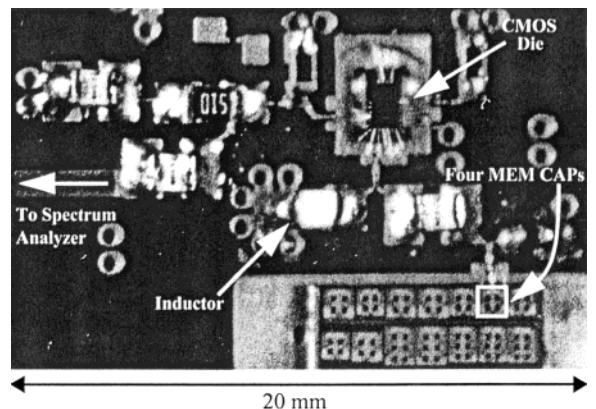
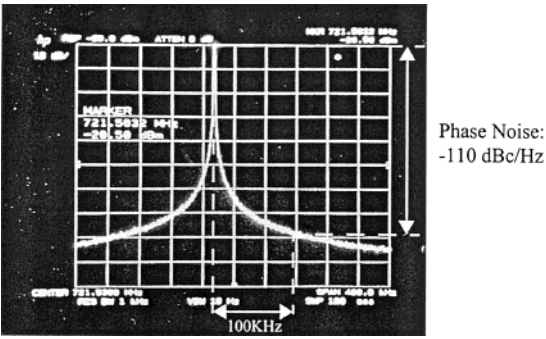


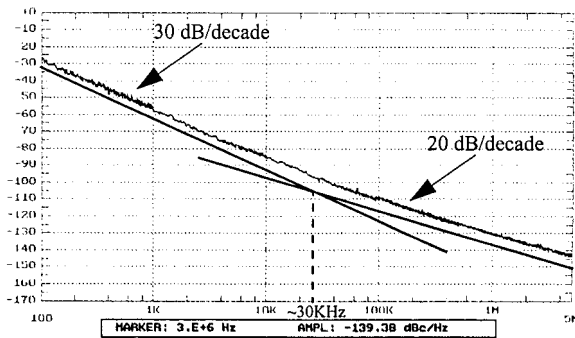
Figure 16. First prototype VCO test board.



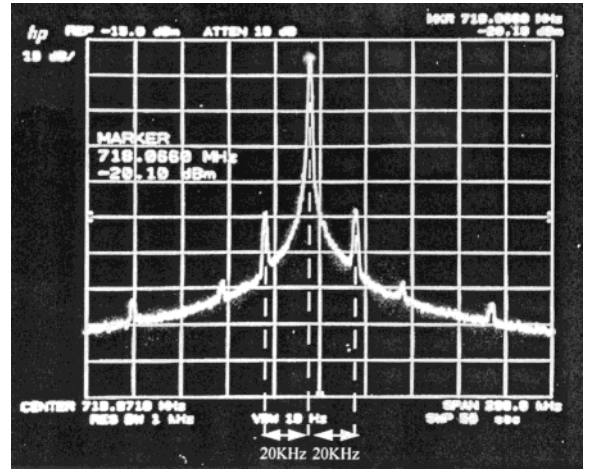
**Figure 17.** First prototype VCO output power spectrum.

high- $Q$  micromachined capacitors and discrete inductor used in the design. The performance is suitable for most wireless communication applications and matches that of typical VCOs relying on external varactor diodes and inductors. The core of the oscillator dissipates 49.5 mW from a 3.3 V power supply. A reduced power consumption is expected from improved device technologies.

From the measurement results obtained in the atmospheric pressure, the VCO phase noise is limited by the  $1/f$  noise from the active circuits for the close-in region with a corner frequency around 30 KHz and thermal noise from the electronics at large offsets rather than the Brownian motion. This is because the total tunable capacitance of 0.8 pF in this design is small compared to the tank parasitic capacitance of approximately 5 pF, 3 pF of which is due to the measurement setup. To verify the pressure-dependent noise shaping effect for the Brownian motion induced phase noise, the VCO is tested in a vacuum environment. Figure 19 presents the oscillator output power spectrum measured in a 20 mT vacuum chamber. The spectrum reveals two main side-band peaks occurring at 20 KHz away from the carrier with a 15 dB noise enhancement. This indicates that the micromachined capacitors have



**Figure 18.** First prototype VCO phase noise plot.



**Figure 19.** First prototype VCO output power spectrum in 20 mT vacuum.

a fundamental mechanical resonant frequency of 20 KHz. The Brownian motion induced phase noise is at least 15 dB higher than the floor at that frequency. The overall phase noise remains the same away from the resonance because it is dominated by noise sources associated with the active electronics in this design. The measured mechanical resonant frequency is less than the designed value of 30 KHz because of the process variations in the deposited film thickness and wet etching rate on the aluminum suspensions. Also shown in Figure 19 are four additional side-band peaks occurring at approximately 40 KHz and 78 KHz away from the carrier each with 5 dB noise enhancement. These peaks are caused by the higher-order mechanical resonances of the micromachined capacitors.

The second prototype VCO replaces the discrete inductor with a three-dimensional coil inductor fabricated on a separate silicon substrate. The three-dimensional inductor has two turns and an inductance of 8.2 nH with a  $Q$  factor of 16 at 1 GHz. Figure 20 presents the photograph of that VCO test board. A set of four parallel-connected micromachined variable capacitors, a three-dimensional coil inductor, and a CMOS VCO electronics die are wire-bonded to form the oscillator. The long alumina bar is used in the prototype inductor fabrication for manual handling. In the future improved process only a small amount of core material is needed, shown by a white box located at the center of the alumina bar, for building the inductor. Because all the key components are fabricated on silicon wafers, they are amenable to integration on the same substrate.

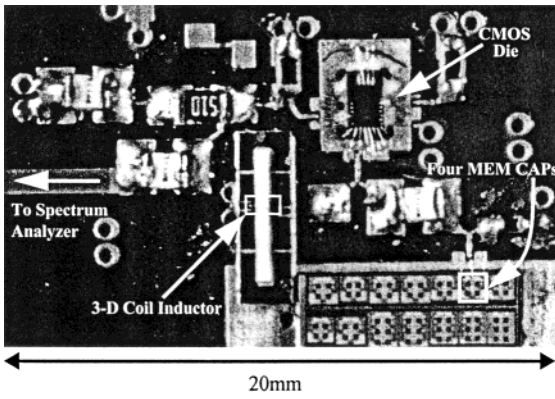


Figure 20. Second prototype VCO test board.

Figure 21 shows the oscillator output power spectrum at 863 MHz with a phase noise of  $-106$  dBc/Hz achieved at 100 KHz offset frequency. The measured phase noise profile is plotted in Figure 22. At 3 MHz offset frequency a phase noise of  $-136$  dBc/Hz is achieved. This phase noise is 3 dB higher than that of the first prototype VCO because of the reduced inductor  $Q$  value. However, the obtained performance is suitable for most wireless communication applications such as GSM cellular telephony and has not been achieved by VCOs relying on conventional silicon junction variable capacitors and spiral inductors. The oscillator is tunable from 851 MHz to 863 MHz with 3 V limited by the parasitics of the test setup.

## VII. CONCLUSION

Micromachining technologies provide IC compatible RF tunable capacitors and three-dimensional coil inductors with high- $Q$  values that cannot be achieved through conventional IC process. These

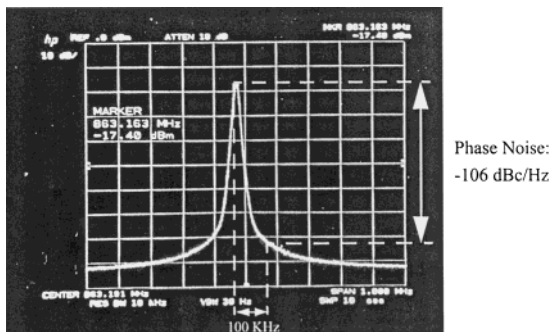


Figure 21. Second prototype VCO output power spectrum.

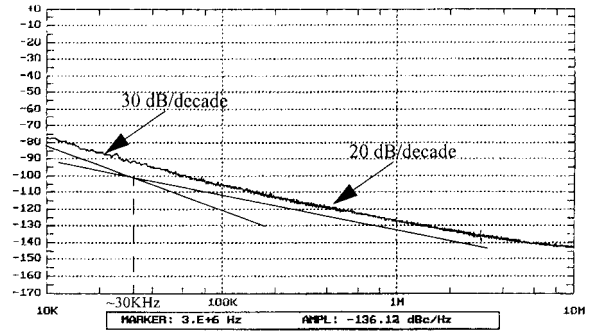


Figure 22. Second prototype VCO phase noise.

high- $Q$  passive components are crucial for integrating high performance RF building blocks, in particular the low phase noise RF VCOs. A prototype RF VCO has been designed and built using the micromachined high- $Q$  tunable capacitors and three-dimensional coil inductor. The oscillator meets the stringent GSM phase noise requirements and demonstrates that complete monolithic high performance VCOs can be achieved through micromachining technologies. Monolithic VCOs will help the size reduction of current wireless transceivers, offering a potential solution to realize a miniature multistandard phone for future wireless communications.

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## BIOGRAPHIES



**Darrin J. Young** earned his B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering and Computer Science at University of California at Berkeley in 1991, 1993, and 1999, respectively. Between 1991 and 1993, he worked at Hewlett-Packard Laboratories in Palo Alto, California, where he designed a shared memory system for a DSP-based

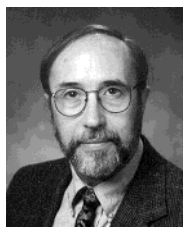
multiprocessor architecture. During the summer of 1997, he worked at Rockwell Semiconductor Systems, where he designed silicon bipolar RF analog circuits for cellular telephony applications. Between 1997 and 1998, he was also at Lawrence Livermore National Laboratory, working on the design and fabrication of three-dimensional RF coil inductors for wireless communications. Dr. Young joined the Department of Electrical Engineering and Computer Science at Case Western Reserve University as an assistant

professor in July 1999. His main research interests include microelectromechanical device design and fabrication, and integrated-circuit design for wireless communications, sensing, biomedical implantation, and general industrial applications.



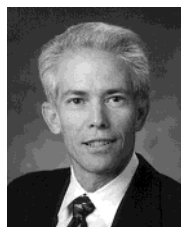
**Bernhard E. Boser** received the Diploma in Electrical Engineering from the Swiss Federal Institute of Technology in 1984 and the M.S. and Ph.D. from Stanford University in 1985 and 1988. From 1988 he was a Member of Technical Staff in the Adaptive Systems Department at AT&T Bell Laboratories. In 1992 he joined the faculty in the Department of Electrical

Engineering and Computer Sciences at the University of California, Berkeley, where he also serves as a Director of the Berkeley Sensor and Actuator Center. Dr. Boser's research is in the area of analog and mixed signal circuits, with special emphasis on micromechanical sensors and actuators. He has served on the program committees of the International Solid-State Circuits Conference, the Transducers Conference, the VLSI Symposium, and was an Associate Editor of the IEEE Journal of Solid-State Circuits.



**Vince Malba** received his Ph.D. in Physical Organic Chemistry from Boston University in September, 1985. His graduate work involved the study of photochemical reaction mechanisms with potential for solar energy storage. As a post-doctoral researcher at Stanford University from 1985 to 1987, he studied gas-phase energy transfer of ions and neutrals.

Dr. Malba joined the Microelectronics Program at LLNL in 1987, developing aluminum-alloy etching processes for VHSIC gate arrays; he is currently a member of the Interconnect Group of the Microelectronics Program, which is investigating laser patterning of three-dimensional surfaces for the production of stacked memories, multichip modules, integrated discretes, and MEM devices. In 1997, he received the Electronic Engineering Technology Division's Outstanding Performance Award. He has published 25 papers and has been awarded 6 patents.



**Anthony Bernhardt** received a B.A. in mathematics at UCLA in 1967 and joined Lawrence Livermore National Laboratory in 1968. From 1973 to 1975, he was a Fannie and John Hertz Foundation Graduate Fellow in Applied Science at the University of California at Davis where he earned a Ph.D. in 1975.

Dr. Bernhardt is Program Leader for Microelectronics at Lawrence Livermore National Laboratory where his recent activities include development of three-dimensional interconnect and cooling technologies for electronic packaging, field emission cathodes for flat panel displays, and three-dimensional inductive components for microelectromagnetic systems. He has led a number of industry-National Laboratory collaborations for the development and commercialization of technologies related to flat panel displays, electronic packaging, and integrated circuits. In 1992 Dr. Bernhardt and two colleagues won the Department of Energy Federal Laboratory Consortium Award for Excellence in Technology Transfer. He has published over 35 papers and holds 14 patents.