Single Crystal 6H-SiC MEMS Fabrication Based On Smart-Cut Technique

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ABSTRACT

A new single crystal silicon carbide MEMS fabrication process is developed using proton-implantation smart-cut technique. A 6H-SiC layer with 1.3 μm thickness has been achieved over an oxidized silicon substrate using the proposed technique. TEM analyses of the silicon carbide thin film reveal single crystal characteristics, which is attractive for potential integration of MEMS devices with high-temperature microelectronics in the same structural layer for harsh environment applications. Implant-induced defect density in the silicon carbide can be substantially reduced to a negligible level through high-temperature annealing. Prototype single crystal 6H-SiC MEMS devices, such as resonators and actuators, have been successfully fabricated as demonstration vehicles for future harsh-environment micro-system implementation.

INTRODUCTION

Single crystal silicon carbide (SiC) material is highly critical for implementing MicroElectroMechanical Systems (MEMS) for high-temperature applications due to its mechanical robustness, chemical inertness, and electrical stability at elevated temperatures [1, 2]. Most MEMS devices require a structural layer over an oxide sacrificial material. Such structures based on SiC have been demonstrated by using single crystal 3C-SiC films, which can be hetero-epitaxially grown on silicon substrates, and wafer bonding techniques to fabricate MEMS sensors for harsh environment applications [3, 4]. However, the 3C-SiC material exhibits a large of amount defects, which is inadequate for building high-performance microelectronic devices, thus hindering potential system integration [5]. In this paper, a new single crystal 6H-SiC MEMS fabrication technology based on proton-implantation smart-cut process is presented. 6H-SiC material is widely used for high-performance microelectronics. Similar techniques have been proposed to produce low-cost silicon on insulator wafers for low-power microelectronics and MEMS applications [6, 7, 8]. At present most MEMS devices call for a structural layer with a thickness of at least 1 μm to achieve desired performance. In this research a single crystal 6H-SiC layer with a thickness of 1.3 μm is demonstrated for MEMS applications. TEM analyses of the resulting SiC layer reveal a negligible implant-induced defect density due to high-temperature annealing and single crystal material characteristics, which are highly desirable for potential integration of MEMS devices with high-temperature sensing and control electronics in the same structural layer for building high-performance harsh-environment micro-systems. Furthermore, the silicon carbide film thickness can

be accurately determined through an implant energy control, which presents a key advantage for high-precision device fabrication. The proposed technique allows an original single crystal 6H-SiC substrate to be reused for the MEMS fabrication process, thus potentially resulting in a significant substrate and processing cost reduction. SiC MEMS prototype devices, such as resonators and actuators with a typical device dimension of a few hundreds of micrometers and a final thickness of 1.2 μm, have been fabricated as demonstrated vehicles for future high-temperature sensors, actuators, and micro-systems implementation. A thicker SiC layer can be obtained by enhancing the implant energy but will be ultimately limited by the equipment capability.

FABRICATION PROCESS

The proposed single crystal SiC MEMS fabrication process flow is presented in Figure 1. The process begins with a commercial 2-inch N-type 6H-SiC wafer from Cree, Inc. The wafer exhibits a thickness of 260 μm with a resistivity of 0.05 Ω·cm and is passivated by a 1000 Å of thermal oxide, which serves as a surface protection layer for wafer handling during the subsequent implant. A proton dosage of $1 \times 10^{17}/cm^2$ has been shown adequate for silicon carbide layer splitting [9] and thus is selected for this experiment. The proton peak concentration location can be controlled by the implant energy. An implant energy of 200 KeV is chosen to achieve an expected H^+ peak concentration of approximately 1.3 μm below the wafer surface, as illustrated in Figure 1a, based on an implant projected range calculation of approximately 65 nm/KeV in silicon carbide. The implanted hydrogen ions introduce micro-cavities along the peak concentration. After bonded to a carrier substrate, the micro-cavities will cause the silicon carbide wafer to split

along the peak concentration by a high-temperature annealing step [9], thus resulting in a single crystal 6H-SiC layer with a thickness of about 1.3 μm over the carrier substrate. This silicon carbide layer thus can be used as a structural material for building high-temperature MEMS sensors and actuators. The silicon carbide thickness can be increased by enhancing the implant energy but is ultimately limited by the equipment capability and processing time. Conventional medium-current implant equipment employed for achieving the required dose range is typically limited to a maximum implant energy of around 400 KeV, corresponding to a thickness of approximately 2.6 μm. Low-current implant equipment can offer higher implant energy but making the processing time and cost prohibitive. In next step, a 4-inch <100> N-type silicon substrate, serving as a carrier wafer, is passivated by a thermal oxide. An oxide thickness of 2 μm is chosen for the prototype fabrication as shown in Figure 1b. After a minor polishing of both wafers surface, the two substrates are extensively cleaned in DI water followed by a reverse RCA cleaning to remove any particles and ionic contaminations and also to obtain hydrophilic surfaces. The two substrates are then brought into contact and initially bonded together at room temperature, followed by an annealing at 300 ^{o}C for 24 hours to maximize the bonding strength as shown in Figure 1c. The bonded wafers are then heated at 1000 ^{o}C for 8 hours to initiate the splitting, causing an approximately 1.3 μm-thick single crystal 6H-SiC layer transferred from the SiC wafer to the silicon substrate, as depicted in Figure 1d. The splitting condition is experimentally determined for the prototype fabrication as a lower temperature process would require an excessive annealing time to initiate the splitting, while a higher temperature annealing may separate the wafers from the bonding interface if the initial bonding is weak. Furthermore, a slow temperature

ramping over one hour is applied to avoid an excessive thermal shock that could also potentially separate the wafers at the oxide interface. After the splitting, the 6H-SiC wafer can be polished and reused by the same procedure to form SiC on insulator (SiCOI) substrates, thus substantially reducing the substrate fabrication cost. At this point, the SiCOI wafer is annealed at 1150 ^{o}C for over 4 hours. This annealing step not only forms a strong chemical bond at the oxide interface but also substantially reduces the implant-induced defects in the transferred SiC layer to a negligible level, as will be illustrated in the following section. An aluminum layer with a thickness of 1000 Å is then sputtered on the SiC surface and patterned to form an etch mask as shown in Figure 1e. The SiC layer is etched using a reactive ion etch employing O_2, CHF_3, and He_2 as etch gases with an etch rate of approximately 250 Å/min. The aluminum layer is then removed with a wet etch as shown in Figure 1f. At this point the wafer is coated by a 1.5 µm-thick photoresist as a protection layer for wafer dicing. After dicing, the photoresist layer is removed followed by releasing MEMS devices in a timed HF etch as depicted in Figure 1g.

FABRICATION AND MEASUREMENT RESULTS

Figure 2 presents an SEM photo of the wafer cross-section after the splitting, showing that a 1.3 µm-thick silicon carbide layer is transferred onto the silicon carrier substrate passivated by a 2.2 µm-thick thermal oxide. The obtained silicon carbide layer achieves a uniform thickness with a variation of 100 Å and a smooth surface. The surface quality is characterized by an atomic force microscope (AFM). Figure 3 presents an AFM three-dimensional surface profile with an average roughness of 4.6 nm. The small surface roughness can be further improved by a minor polishing step to obtain a high quality surface.

TEM analyses have been performed to analyze the silicon carbide material characteristics before and after the splitting. Figure 4 shows a dark field TEM cross-section image of an as-implanted silicon carbide wafer. From the figure, it can be seen that a localized implant-induced highly damaged silicon carbide region with a width around 200 nm is located at approximately 1.3 μm below the silicon carbide surface. This damaged layer causes the wafer to split when annealed at elevated temperatures. The implant-induced defect density decreases toward the surface and is estimated as $10^{12}/cm^2$, $2 \times 10^{11}/cm^2$, and $4 \times 10^{10}/cm^2$ at 0.1 μm, 0.2 μm, and 0.3 μm away from the center of the damaged region, respectively. The defect density can be significantly reduced by the subsequent high-temperature splitting and annealing process. Figure 5a presents a corresponding dark field TEM cross-section image of a split SiC material indicating that a thin oxide layer of 0.09 μm is formed at the wafer surface caused the high-temperature splitting process conducted in an oxygen environment, thus resulting in a 1.3 μm-thick SiC layer. The high-temperature splitting can also be performed in a non-oxygen environment to avoid the surface oxidation. A detailed inspection reveals a thin defect region with a thickness around 40 nm between the surface oxide and the split SiC layer as shown in Figure 5b with estimated defect densities of $2 \times 10^{11}/cm^2$ and $5 \times 10^{10}/cm^2$ at 0.2 μm and 0.3 μm away from the wafer surface, respectively. The subsequent annealing step at 1150 ^{o}C substantially reduces the implant-induced defects in the SiC layer to a negligible level. Figures 6a presents the dark field TEM cross-section image of the same split SiC layer after the annealing, showing a final SiC layer thickness of 1.2 μm with a 0.2 μm of surface oxide due to further oxidation. Figure 6b shows a close view of the interface between the surface oxide and the split SiC layer. A thin defect region less than 10 nm is visible along the interface.

However, the TEM of the SiC region underneath is indistinguishable from that of the original single crystal 6H-SiC substrate. The surface oxide can be removed by HF followed by a minor polishing process to eliminate the residual defect region to obtain a high quality silicon carbide layer. Figure 7 presents a selected area electron diffraction pattern (SAD) of the split silicon carbide material. The diffraction pattern indicates single crystal characteristics, which is critical for realizing high-performance MEMS devices and potential system integration with high-temperature microelectronics in the same structural layer for harsh environment applications.

A number of prototype microstructures such as resonators and actuators have been successfully fabricated using the proposed fabrication technology. Figure 8a presents an SEM photo of a fabricated 6H-SiC micro-resonator. The device exhibits a length of 450 μm with a beam width of 4.5 μm and comb finger spacing of 2.5 μm. A close view of the comb fingers and proof mass are shown in Figure 8b. The resonator is freely released from the substrate with an underneath 2.2 μm of air gap. The demonstrated MEMS structures can be used as building blocks to design and fabricate more complex micro-systems for harsh environment applications in the future.

CONCLUSIONS

A single crystal 6H-SiC MEMS fabrication technology has been demonstrated using proton-implantation smart-cut technique. Prototype MEMS resonators and actuators have been successfully fabricated as demonstration vehicles for future high-performance harsh-environment micro-system implementation. The proposed technique allows an original single crystal 6H-SiC substrate to be reused for the MEMS fabrication process, thus potentially resulting in a significant

substrate and processing cost reduction. Material analyses show that the transferred silicon carbide layer reveals single crystal characteristics and exhibits a negligible defect density after high-temperature annealing. These characteristics are critical for realizing high-performance MEMS sensors, actuators, and potential system integration with high-temperature microelectronics in the same structural layer. The proposed technology is also attractive for potentially realizing other single crystal thin films, such as GaAs and GaN, on an insulated carrier substrate for integrating micro-systems with optoelectronics.

ACKNOWLEDGMENT

The fabrication process was performed at Micro-Fabrication Laboratory at Case Western Reserve University.

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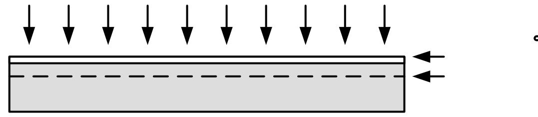

Figure 1a. Proton Implantation

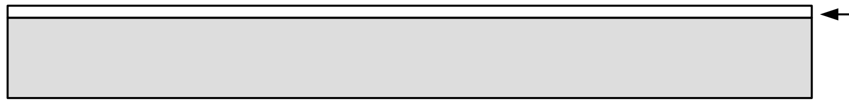

Figure 1b. Oxidizing Silicon Carrier Wafer

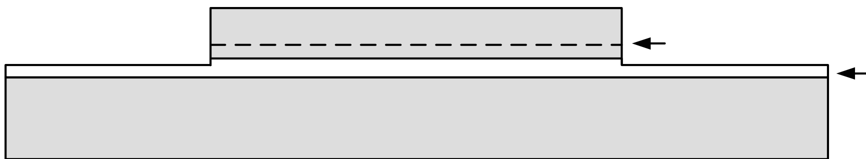

Figure 1c. Wafer Bonding

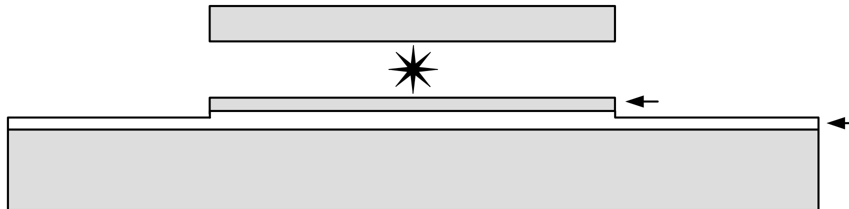

Figure 1d. SiC Wafer Splitting

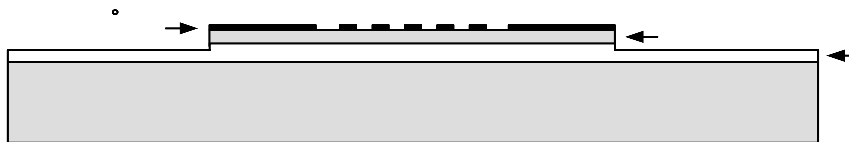

Figure 1e. Aluminum Deposition and Patterning

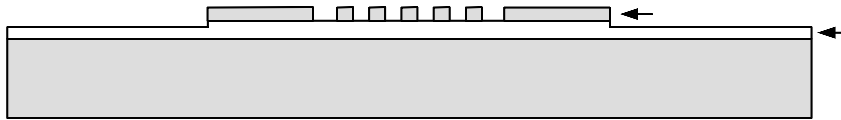

Figure 1f. Split SiC Layer Etching

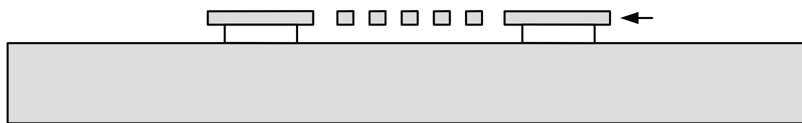

Figure 1g. Released Microstructure

Figure 1. Single Crystal Silicon Carbide MEMS Process

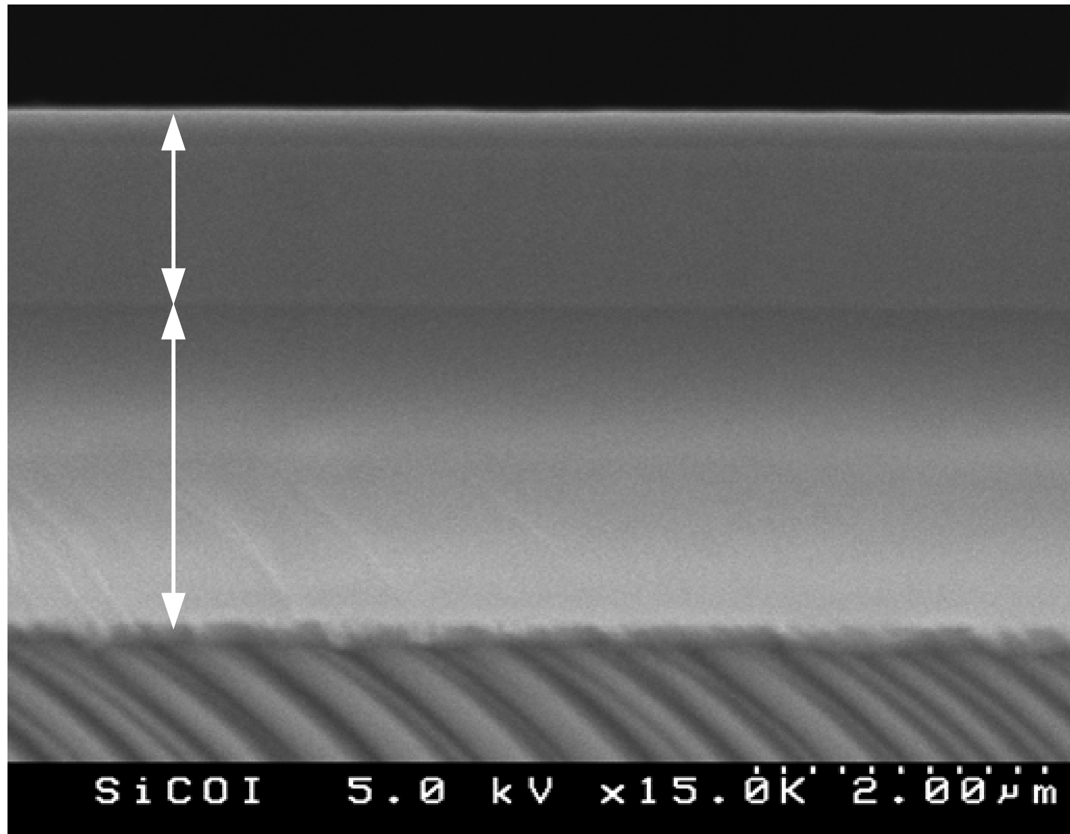

Figure 2. Wafer Cross-Sectional View After Splitting

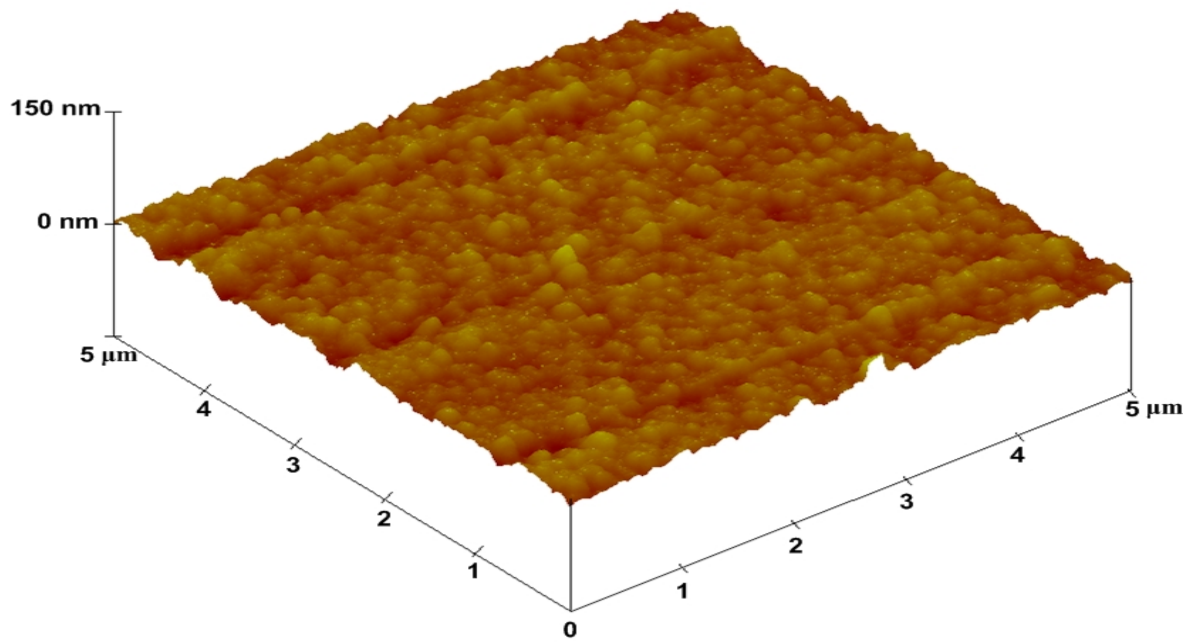

Figure 3. AFM Three-Dimensional Surface Profile

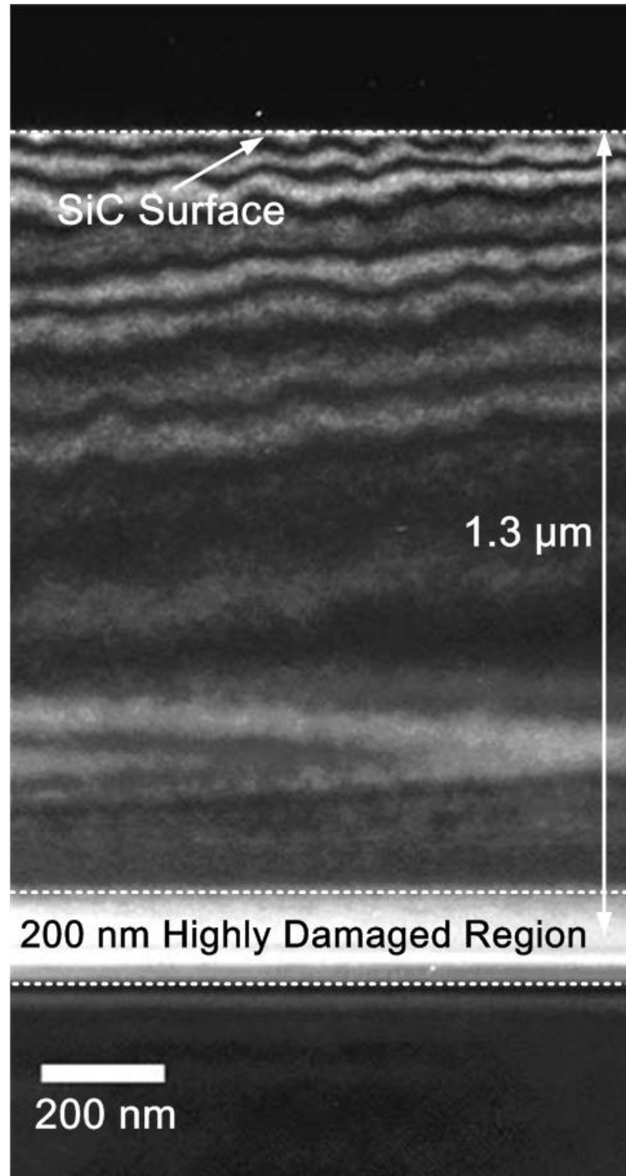

Figure 4. Dark Field TEM of As-Implanted SiC Cross Section

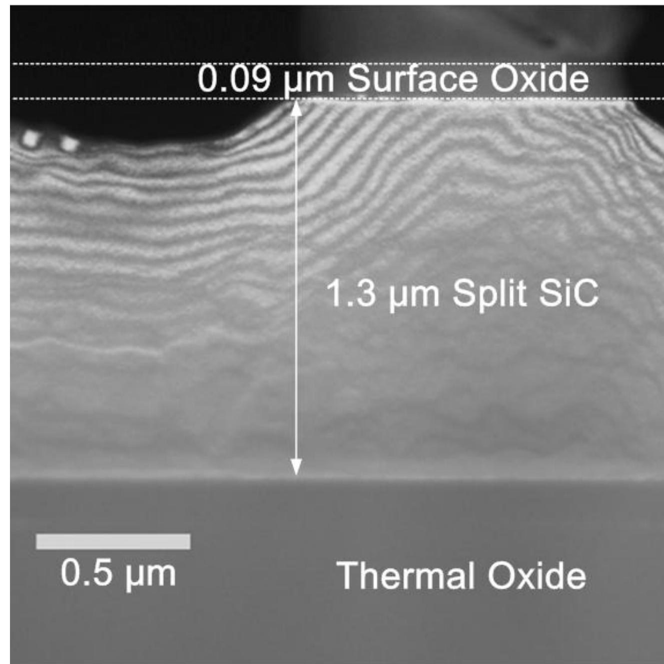

Figure 5a. TEM of Split SiC Cross Section

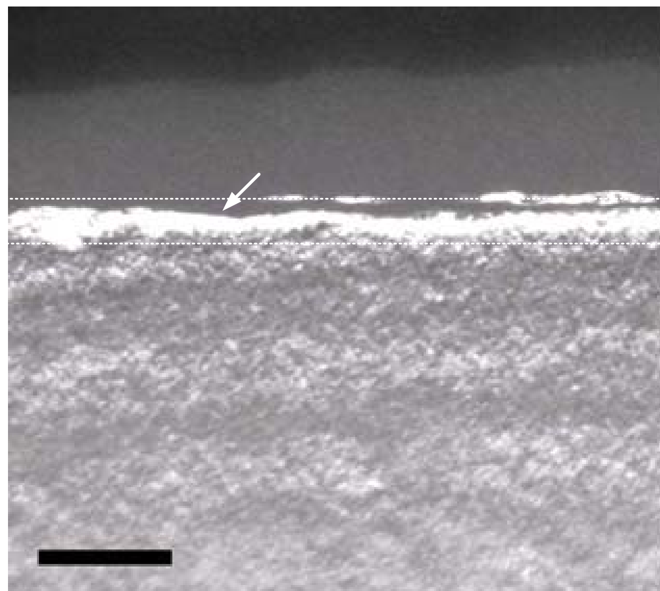

Figure 5b. TEM of Interface Between Split SiC and Surface Oxide

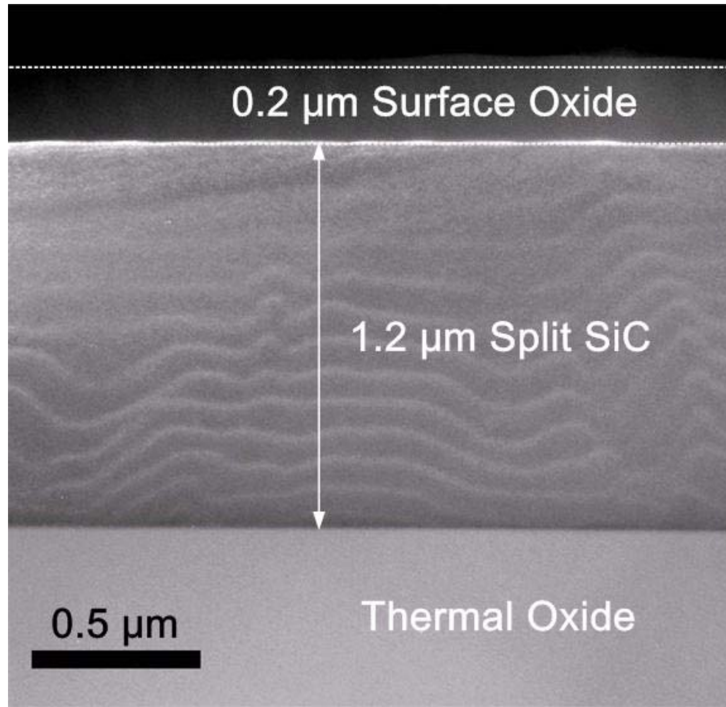

Figure 6a. TEM of Annealed Split SiC Cross

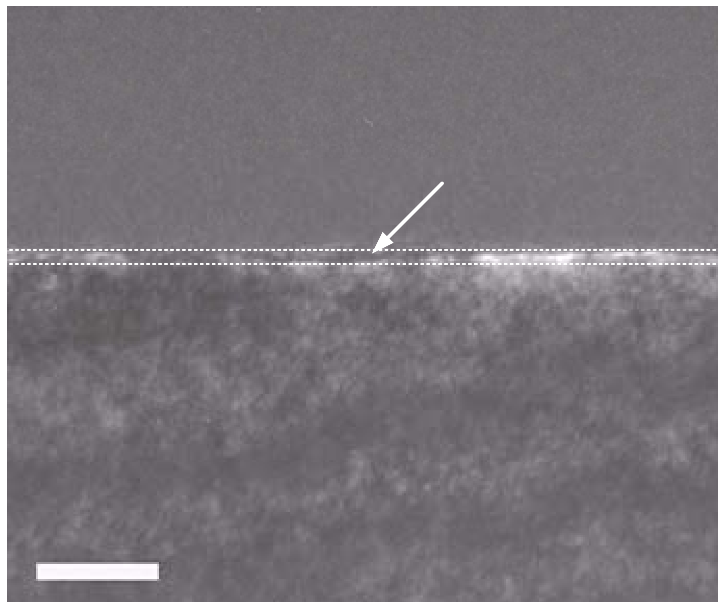

Figure 6b. TEM of Interface Between Annealed Split SiC and Surface Oxide

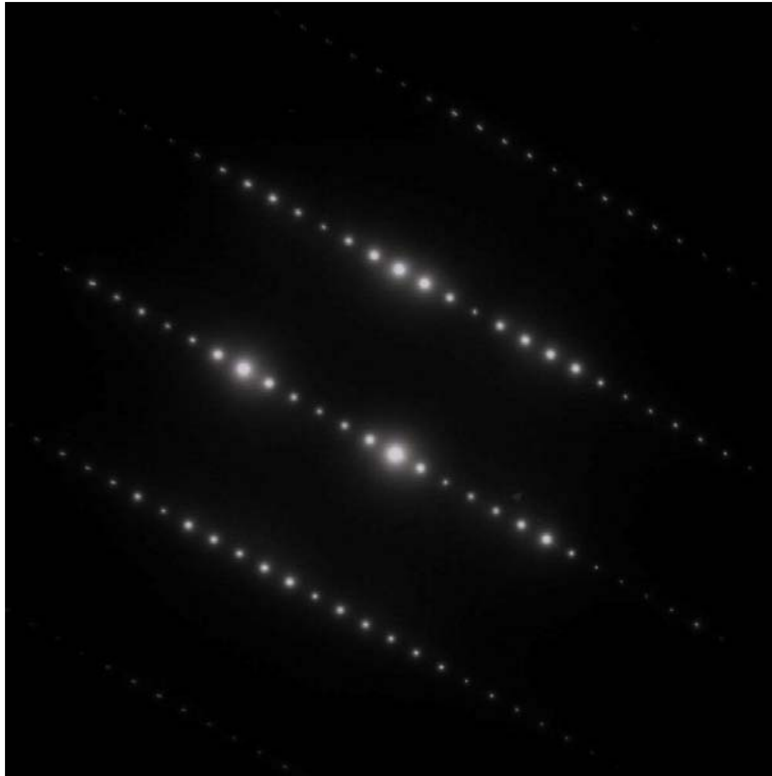

Figure 7. SAD of the Split SiC Layer

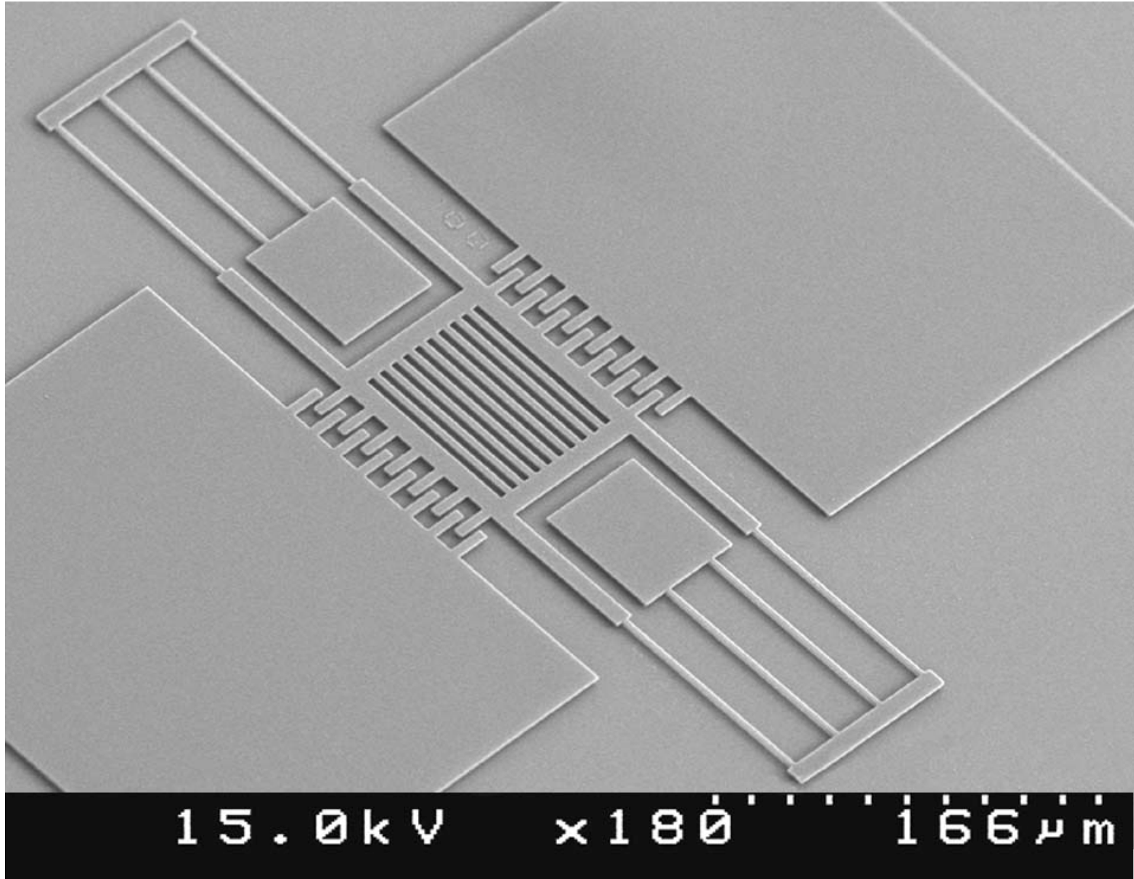

Figure 8a. Fabricated 6H-SiC Resonator Top View

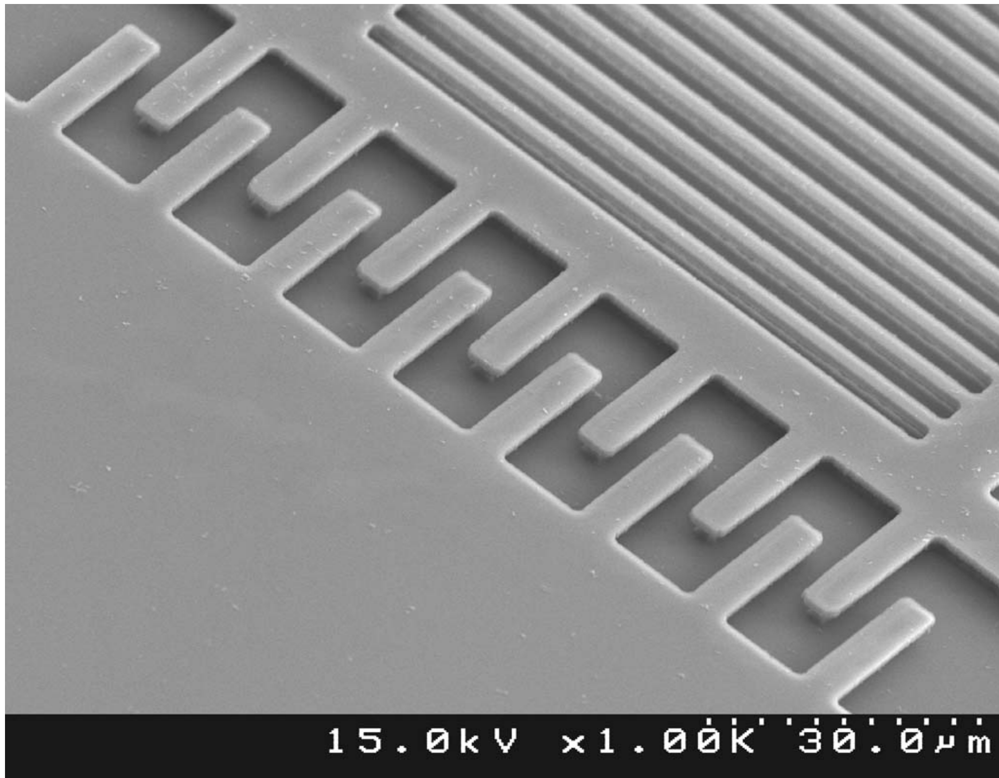

Figure 8b. Resonator Comb Fingers and Proof Mass